A SYCL COMPILER AND RUNTIME ARCHITECTURE
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And many more!
Agenda

• What is SYCL?
• “Hello, world!” in SYCL
• Scheduler
• Compilation flow
• SPIR-V
• Integration header
• Upstream plan
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What is SYCL?

SYCL is a cross platform abstraction layer for heterogeneous compute developed by the Khronos Group.

It allows code for heterogeneous processors (CPU, GPU, FPGA, etc.) to be written in a “single-source” style using standard C++11.

https://www.khronos.org/sycl/
“Hello, world!”

template <typename T>
void vector_add(const std::vector<T>& A, const std::vector<T>& B, std::vector<T>& C) {
    deviceQueue.submit([&](handler& cgh) {
        auto accessorA = bufferA.get_access<sycl_read>(cgh);
        auto accessorB = bufferB.get_access<sycl_read>(cgh);
        auto accessorC = bufferC.get_access<sycl_write>(cgh);

        cgh.parallel_for<class vec_add>(range<1>(A.size())),
        [=](id<1> wiID) {
            accessorC[wiID] = accessorA[wiID] + accessorB[wiID];
        });
    });
}
Intel’s Compiler and Runtime for SYCL

Intel SYCL

SYCL Runtime

Device Management
Scheduler
Error Checking
Data Management

SYCL Device Compiler

OpenCL
Your Favorite Runtime

Note: Boxes not to scale
Note: Not yet 100% conformant
SYCL standard library

SYCL standard library implementation consists of 28 public headers, and ~30 implementation (detail) headers:

- include/CL/sycl/accessor.hpp
- include/CL/sycl/buffer.hpp
- include/CL/sycl/device.hpp
- include/CL/sycl/kernel.hpp
- etc.
SCHEDULER
Scheduler

deviceQueue.submit([&](handler& cgh) {
    auto accessorA = bufferA.get_access<sycl_read>(cgh);
    auto accessorB = bufferB.get_access<sycl_read>(cgh);
    auto accessorC = bufferC.get_access<sycl_write>(cgh);

    cgh.parallel_for<class kernel_1>(range<1>(A.size()),
    [=](id<1> wiID) {
        accessorC[wiID] = accessorA[wiID] + accessorB[wiID];
    });
});
Scheduler

deviceQueue.submit([&](handler& cgh) {
    auto accessorA = bufferA.get_access<sycl_read>(cgh);
    auto accessorB = bufferB.get_access<sycl_read>(cgh);
    auto accessorC = bufferC.get_access<sycl_write>(cgh);

    cgh.parallel_for<class kernel_1>(range<1>(A.size()),
        [=](id<1> wiID) {
            accessorC[wiID] = accessorA[wiID] + accessorB[wiID];
        });
});

deviceQueue.submit([&](handler& cgh) {
    auto accessorC = bufferC.get_access<sycl_read>(cgh);
    auto accessorD = bufferD.get_access<sycl_read>(cgh);
    auto accessorE = bufferE.get_access<sycl_write>(cgh);

    cgh.parallel_for<class vec_add>(range<1>(C.size()),
        [=](id<1> wiID) {
            accessorE[wiID] = accessorC[wiID] + accessorD[wiID];
        });
});
Scheduler

deviceQueue.submit([&](handler& cgh) {
    auto accessorA = bufferA.get_access<sycl_read>(cgh);
    auto accessorB = bufferB.get_access<sycl_read>(cgh);
    auto accessorC = bufferC.get_access<sycl_write>(cgh);

    cgh.parallel_for<class kernel_1>(range<1>(A.size()),
        [id=1](id<1> wiID) {
            accessorC[wiID] = accessorA[wiID] + accessorB[wiID];
        });
});

deviceQueue.submit([&](handler& cgh) {
    auto accessorC = bufferC.get_access<sycl_read>(cgh);
    auto accessorD = bufferD.get_access<sycl_read>(cgh);
    auto accessorE = bufferE.get_access<sycl_write>(cgh);

    cgh.parallel_for<class vec_add>(range<1>(C.size()),
        [id=1](id<1> wiID) {
            accessorE[wiID] = accessorC[wiID] + accessorD[wiID];
        });
});

No explicit “wait” operation! SYCL runtime is responsible for synchronization.
What do you mean everyone doesn't hack on Compilers for fun?
Standard C++ flow

a.cpp

clang -c

a.o

ld

a.out
Standard C++ flow => SYCL flow

1. `a.cpp` -> `clang -c -fsycl`
2. `a.o` -> `ld -lsycl`
3. `a.out`
SYCL compilation flow (under the hood) *

Device compilation:
- a.cpp
  - clang -fsycl-is-device -int-header=...
- a.device.ll
- a.int.header.h
- a.device.bin (SPIR-V)

< device compiler >

Host compilation:
- a.host.ll
- a.host.o
- ld -lsycl
- a.o
- a.out

* simplified
SYCL compilation flow (under the hood) *

Device compilation

```
c.l -fsyju-is-device -int-header=...  
c.cpp
```

Host compilation

```
c.l -include=a.int.header.h
```

```
cpp
```

```
< device compiler >
```

```
ap.device ll
```

```
ap.int.header.h
```

```
ap.device.bin (SPIR-V)
```

```
ap.host.ll
```

```
ap.host.o
```

```
ap.o
```

```
ld -1sycl
```

```
ap.out
```

* simplified

* Other names and brands may be claimed as the property of others.
SPIR-V support

SPIR-V is a device-agnostic IR originally created for OpenCL and Vulkan.

It allows to run a single SYCL executable on any device that supports SPIR-V.

SPIR-V Translator from LLVM IR to SPIR-V is developed on Github: https://github.com/KhronosGroup/SPIRV-LLVM-Translator
SYCL flow: integration header

cgh.parallel_for<class kernel_1>(cl::sycl::range<1>(8),
    [=](cl::sycl::id<1> wiID) {
        accessorC[wiID] = accessorA[wiID] + accessorB[wiID];
    });

Step 1: device compiler extracts the lambda function.

Class name `kernel_1` is a device kernel name.
SYCL flow: integration header

cgh.parallel_for<class kernel_1>(cl::sycl::range<1>(8),
   [=](cl::sycl::id<1> wiID) {
      accessorC[wiID] = accessorA[wiID] + accessorB[wiID];
   });

Step 1: device compiler extracts the lambda function.

Class name `kernel_1` is a device kernel name.

a.device.bin:

___kernel kernel_1(T* buf) {
   ...
}
SYCL flow: integration header

cgh.parallel_for<class kernel_1>(cl::sycl::range<1>(8),
[=](cl::sycl::id<1> wiID) {
   accessorC[wiID] = accessorA[wiID] + accessorB[wiID];
});

Step 2: Host code must call the device function by name, and provide the required parameters.

a.host.cpp:

clCreateKernel("kernel name");
clSetKernelArg(0, buf);

a.device.bin:

__kernel kernel_1(T* buf) {
   ...
}
SYCL flow: integration header

cgh.parallel_for<class kernel_1>(cl::sycl::range<1>(8),
    [=](cl::sycl::id<1> wiID) {
        accessorC[wiID] = accessorA[wiID] + accessorB[wiID];
    });

No way to map a type name (kernel_1) to a string!

a.host.cpp:
clCreateKernel("kernel name");
clSetKernelArg(0, buf);

a.device.bin:
__kernel kernel_1(T* buf) {
    ...
}
SYCL flow: integration header

cgh.parallel_for<class kernel_1>(cl::sycl::range<1>(8),
    [=](cl::sycl::id<1> wiID) {
        accessorC[wiID] = accessorA[wiID] + accessorB[wiID];
    });

a.host.cpp:

clCreateKernel("kernel name");
clSetKernelArg(0, buf);

a.device.bin:

__kernel kernel_1(T* buf) {
    ...}

No way to determine an order of arguments captured by a lambda.
SYCL flow: integration header

cgh.parallel_for<class kernel_1>(cl::sycl::range<1>(8),
    [=](cl::sycl::id<1> wiID) {
        accessorC[wiID] = accessorA[wiID] + accessorB[wiID];
    });

a.int.h:

    template<>
    class KernelDesc<kernel_1> {
        const char* getName();
        unsigned getArgNum();
        ArgDesc getArg(unsigned);
    };

a.host.cpp:

    clCreateKernel(
        KernelDesk<T>::getName());
    ...

a.device.bin:

    __kernel kernel_1(T* buf) {
        ...
    }
SYCL upstream to LLVM.org

• Intel/llvm repository is a staging area to design concepts and prototype solutions

• Contribution to llvm.org is our primary goal
  • First changes to the clang driver are already committed: https://reviews.llvm.org/D57768
  • Detailed plan for upstream: https://github.com/intel/llvm/issues/49
  • SYCL source code: https://github.com/intel/llvm/tree/sycl
Call to action

We welcome feedback and input on the design and implementation.

Please contribute ideas/implementation to our sandbox or join us on the path to llvm.org!

https://github.com/intel/llvm