

Debugging And Optimizing OpenCL* Applications

Best Practices and Tools

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Objectives

- Understand the architecture characteristics relevant to compute applications on Intel® Processor Graphics
- Learn techniques for optimizing OpenCL* applications for Intel® Processor Graphics
- Introduce with Intel® tools for development, debugging and optimizing OpenCL* applications



Agenda

- Intel® Processor Graphics introduction
- Optimization techniques for OpenCL* applications
- Develop OpenCL* applications with Intel® SDK for OpenCL[™] Applications
- Debug OpenCL* applications with Intel® SDK for OpenCL[™] Applications
- Optimize OpenCL* application with Intel tools
 - Intel® VTune™ Amplifier XE
 - Intel® SDK for OpenCL* Applications



Intel® Processor Graphics

Introduction

Intel® Processor Graphics Architecture

- Today, our focus is on Intel® Iris[™] Graphics and Intel® HD Graphics in 6th Generation Intel® Core[™] Processors
 - Or, Intel Processor Graphics Gen9
- For more details, see our whitepaper, The Compute Architecture of Intel Processor Graphics Gen7.5/Gen8.0/Gen9.0
- <u>https://software.intel.com/en-us/articles/intel-</u> graphics-developers-guides



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Intel® Processor Graphics Architecture

- Outstanding rendering and media performance
- High-throughput general purpose compute capabilities
- High bandwidth memory hierarchy
- Deep integration with on-die CPUs and other SoC devices



Intel® Processor Graphics Architecture

- Modular architecture
- Scalability for a range of products





GEN9 Core Processor



An Intel® Core™ i7 processor 6700K SoC and its ring interconnect architecture.





Intel® Graphics Architecture Building Blocks



- Modular architecture, which enables scalability across a wide range of target products

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Intel® Graphics Architecture Building Blocks

A potential product design composed of three slices, each with three subslices, for a total of 72 EUs



Intel® Core™ i7-6970HQ Processor with Intel® Iris™ Pro Graphics 580



Intel® Graphics Architecture Building Blocks - EU

- 7 threads with
 - 128 GRF of 32 bytes, Accessible as SIMD-8 32bit
- Can co-issue up to 4 instruction processing units including:
 - 2 FPUs
 - Branch unit
 - Message send unit



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Intel® Graphics Architecture Building Blocks - Subslice

- 8 EUs (can be changed for scalability) X 7 threads
 - Dedicated hardware resources and register files for 56 simultaneous threads
- Local thread dispatcher unit
- Supporting instruction caches
- Sampler
 - Read-only memory fetch unit includes 2-level caches
- Data port
 - A memory load/store unit





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Intel® Graphics Architecture Building Blocks - Slice

- 3 sub-slices for a total of 24 EUs



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Intel® Graphics Architecture Building Blocks - Slice

- Banked L3 cache
 - Cachelines are 64 bytes each
- Smaller highly-banked shared local memory
 - For sharing among EU hardware threads within the same subslice
 - Same latency as L3 data cache
 - Can yield full bandwidth for access patterns that may not be 64-byte aligned



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Intel® Graphics Architecture Building Blocks - Product

- SoC product instantiates a single slice or groups of slices.
- Additional front end logic
 - Manage command submission
- Fixed-function logic
 - Support 3D rendering, and media pipelines
- Graphics technology interface (GTI)
 - Interfaces to the rest of the SoC components (memory, CPU, ...)



The Intel® Core™ i7 processor 6700K with Intel® HD Graphics 530.

Intel® Graphics Architecture - Memory

- Share DRAM physical memory with the CPU
 - Zero copy
- Shared memory coherency and consistency



SoC chip level memory hierarchy and its theoretical peak bandwidths for Intel processor graphics gen9.

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How OpenCL* Maps To Intel® Processor Graphics

Executing OpenCL* Kernels

- OpenCL* work items map to SIMD lanes of a hardware thread
- Compiler may decide to compile a kernel SIMD32, SIMD16, or SIMD8
 - A compiler heuristic will choose a SIMD width that best maximizes register footprint within a single hardware thread and avoid needs for register spill/fill.
 - Typically short kernels that need less than 128 bytes of private memory will compile to SIMD32



Executing OpenCL* Kernels



Compiler can trade register space for IPC!

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Executing OpenCL* Kernels

Example: SIMD16 compile, 64 work items per work group



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Optimize OpenCL* applications

Best Practices

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Two Levels of Optimizations for OpenCL*

- Application level optimization
 - Optimization is ~vendor agnostic, tools are ~similar
 - Many API level tricks are ~portable
- Kernel level optimization side
 - Entirely vendor-specific (and so are tools)
 - Kernels optimizations are generally less portable







- Optimize host API calls
- Reduce host <> device memory traffic and bandwidth
- Optimizing memory access
- Maximizing occupancy and computation
- Kernel algorithm optimization

OpenCL* Developer Guide for Intel® Processor Graphics: https://software.intel.com/en-us/iocl_opg





- Optimize host API calls
- Reduce Host <> Device memory traffic and bandwidth
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ANALYZE Intro to Host-Side API Optimization

- "Wall-clock" time: wrap OpenCL* API calls with timestamps + printfs
 - Most "device" OpenCL* APIs (like clEnqueueNDRangeKernel) just put a call into a queue and immediately return
 - To measure actual execution time, need to synchronize on completion
- Better solution with profiling events
 - OpenCL* profiling info from events associated with all queued commands:
 - Time spent in the command queue, driver and actual hardware exec
 - Enable queue for profiling with CL_QUEUE_PROFILING_ENABLE
 - Wait for the command completion before querying the event stats
- Best solution
 - Use Intel® Code Builder to get API profiling report and optimization tips

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Avoid Redundant Usage of API Calls



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Reusing Compilation Results

- Reusing compilation results is typically faster than recreating the program from the source
 - Check it for your specific program and device
- Cache the resulting binaries after the first OpenCL* compilation and reuse them by calling clCreateProgramWithBinary
 - To retrieve binaries generated from CreateProgramWithSource and clBuildProgram:
 - Call clGetProgramInfo with the CL_PROGRAM_BINARIES parameter
- A better way Pre compile your program offline with Intel® Code Builder for OpenCL[™] API and save intermediate binaries



II	Se	ssion Info	Host Profiling Kernels		Overview 4		
<u>pi Calls:</u> [Data Table] G	raphical View	inefficient "clCreateBuffer" calls. The host program includes 10 calls to "clCreateBuffer" where "flags" includes "CL_MEM_COPY_HOST_PTR".					
Api Name	Count	# Errors	Total Duration (µs)	Avg Duration (µs)	4 redundant calls to "clCrea The host program includes 5 calls to	ateContextFromType". o "clCreateContextFromType" with the sam	
clBuildProgram	5	0	1800529.69	360105.938	arguments.		
clCreateBuffer	15	0	605422.278	40361.485	4 redundant calls to "clCreateCommandQueue". The host program includes 5 calls to "clCreateCommandQueue" that refer t same device: "Device [1] (Intel(R) HD Graphics 4400)". "clEnqueueReadBuffer" calls. The host program includes 5 calls to "clEnqueueReadBuffer".		
clCreateCommandQueue	5	0	42899.852	8579.97			
clCreateContextFromType	5	0	73049.299	14609.86			
clCreateKernel	5	0	1173.758	234.752			
clCreateProgramWithSource	5	0	491.837	98.367			
clEnqueueNDRangeKernel	5	0	560.809	112.162	94.857	124.390	
clEnqueueReadBuffer	5	0	175029.128	35005.826	30261.938	43323.538	
clFinish	10	0	308955.786	30895.579	0.821	123338.613	
clGetDeviceIDs	5	0	10.264	2.053	1.232	2.874	
clGetPlatformIDs	2	0	47.213	23.607	0.411	46.803	
clGetPlatformInfo	10	0	16.422	1.642	0.411	5.337	
clReleaseCommandQueue	5	0	19446.86	3889.372	348.556	9850.7	
clReleaseContext	5	0	15139.796	3027.959	2651.322	3382.919	
clReleaseDevice	5	0	15.19	3.038	2.053	3.695	
clReleaseKernel	5	0	27.917	5.583	4.927	6.569	
clReleaseMemObject	15	0	256074.68	17071.645	14939.038	22415.946	

Optimization Notice

Code Builder

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	Ses	ssion Info	E Host Profiling	Kernels	Overview	
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- Optimize host API calls
- Reduce Host <> Device memory traffic and bandwidth
- Optimizing memory access
- Maximizing occupancy
- Maximizing computation
- Kernel algorithm optimization





- The key hardware feature that enables zero copy is the fact that the CPU and GPU have shared *physical* memory
- Memory shared between the CPU and GPU can be efficiently accessed by both devices







- Always improves performance
- To create zero copy buffers, do one of the following:
 - Use CL_MEM_ALLOC_HOST_PTR
 - Let the runtime handle creating a zero copy allocation buffer for you
 - Use CL_MEM_USE_HOST_PTR with:
 - Buffer allocated at a 4096 byte boundary (aligned to a page and cache line boundary)
 - Total size that is a multiple of 4096 byte (page size)

int *pbuf = (int *)_aligned_malloc(sizeof(int) * 1024, 4096); cl_mem myZeroCopyCLMemObj = clCreateBuffer(ctx,...CL MEM USE HOST PTR...);

https://software.intel.com/en-us/articles/getting-the-most-from-opencl-12-how-to-increase-performance-by-minimizing-buffer-copies-on-intel-processor-graphics

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Zero Copy - Accessing the Buffer on the Host

- Use clEnqueueMapBuffer() and clEnqueueUnmapMemObject()
- Don't use:
 - clEnqueueReadBuffer()
 - clEnqueueWriteBuffer()
- * This behavior may not be the same on all platforms.



		•	•			
	Se	ssion Info	Host Profiling	Kernels (Overview	<u> </u>
Api Calls: [Data Table]	Graphical View				inefficient "clCreateBuffer" The host program includes 10 calls "CL_MEM_COPY_HOST_PTR".	calls. to "clCreateBuffer" where "flags" includes
Api Name	▲ Count	# Errors	Total Duration (µs)	Avg Duration (µs)	4 redundant calls to "clCrea The host program includes 5 calls to	ateContextFromType".) "clCreateContextFromType" with the sam
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+ clCreateCommandQueue	5	0	42899.852	8579.97		
+ clCreateContextFromType	5	0	73049.299	14609.86	same device: Device [1] (Intel(R) HD Graphics 4400) . "clEnqueueReadBuffer" calls. The host program includes 5 calls to "clEnqueueReadBuffer".	
+ clCreateKernel	5	0	1173.758	234.752		
+ clCreateProgramWithSource	5	0	491.837	98.367		
+ clEnqueueNDRangeKernel	5	0	560.809	112.162	"clCreateBuffer" calls where "host_ptr" isn't 4K aligned. The host program includes 44 calls to "clCreateBuffer" where "host_ptr" is 4K aligned. "clCreateBuffer" calls where "size" isn't a multiple of 64 bytes. The host program includes 22 calls to "clCreateBuffer" where "size" is not a multiple of 64 bytes.	
+ clEnqueueReadBuffer	5	0	175029.128	35005.826		
+ clFinish	10	0	308955.786	30895.579		
+ clGetDeviceIDs	5	0	10.264	2.053		
+ clGetPlatformIDs	2	0	47.213	23.607		
+ clGetPlatformInfo	10	0	16.422	1.642	"clEnqueueWriteBuffer" calls. The host program includes 12 calls to "clEnqueueWriteBuffer".	
+ clReleaseCommandQueue	5	0	19446.86	3889.372		
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Code Builder
Code Builder API Calls Report

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Api Calls: [Data Table] Gra	There a	re two v	vays to ensure zero-co	× opy path		inefficient "clCreateBuffer" The host program includes 10 call "CL_MEM_COPY_HOST_PTR"	" calls. s to "clCreateBuffer" where "flags" includes		
Api Name	on men memor	nory obj y with "(thod en	ects mapping. Allocat CL_MEM_ALLOC_HOS sures that the memor	e T_PTR", v is	(µs)	4 redundant calls to "clCre The host program includes 5 calls arguments.	eateContextFromType". to "clCreateContextFromType" with the same		
+ clCreateBuffer + clCreateCommandQueue + clCreateContextEromType	efficient is to all	tly mirro ocate pr	ored on the host Anot operly aligned and size	her way . .ed		4 redundant calls to "clCre The host program includes 5 calls same device: "Device [1] (Intel(R)	eateCommandQueue". to "clCreateCommandQueue" that refer to the) HD Graphics 4400)".		
+ clCreateKernel + clCreateProgramWithSource	the Ope	y yourse enCL fra	If and share the point mework by using the	er with		"clEnqueueReadBuffer" ca The host program includes 5 calls	lls. to "clEnqueueReadBuffer".		
+ clEnqueueNDRangeKernel + clEnqueueReadBu	CL_ME			20905 570		"clCreateBuffer" calls where The host program includes 44 call 4K aligned.	e " host_ptr" isn't 4K aligned. s to "clCreateBuffer" where "host_ptr" is not		
+ cleatDeviceIDs	+ critish For best results, align memory address to					"clCreateBuffer" calls where "size" isn't a multiple of 64 bytes.			
+ clGetPlatformIDs	bry page (4	c bytes).		23.607		The host program includes 22 call	s to "clCreateBuffer" where "size" is not a		
+ clGetPlatformInfo	10		10.422	1.642		шицріе от 04 бутез.			
+ clReleaseCommandQueue	5	0	19446.86	3889.372		"clEnqueueWriteBuffer" cal	lls. s to "clEnqueueWriteBuffer"		
+ clReleaseContext	5	0	15139.796	3027.959		ine nost program includes 12 calls to "clEnqueueWriteBuffer".			
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Code Builder Shared Virtual Memory (SVM)

- Supported from OpenCL* 2.0
- Enables the host and device to seamlessly share pointers and complex pointer-containing data-structures
 - Linked lists or trees
- Tight Host-Kernel synchronization using atomics
 - Just like two distinct cores in a CPU



Code Builder Shared Virtual Memory (SVM)

- Basically a productivity feature
 - Targeted to fulfill the needs of developers for tighter host-device synchronization beyond enqueuing commands and synchronizing through events
- Also a very important performance feature
 - Go to "GPU daemon Road to Zero Cost Submission"

by Michal Mrozek and Zbigniew Zdanowicz (Intel) on THURSDAY 21st APRIL 16:30 – 17:00



Code Builder Shared Virtual Memory (SVM)

- Requires dedicated hardware coherency support
 - Such as enabled in Intel Core Processors with Intel® Graphics Gen8/Gen9 compute architecture
- There are different levels of SVM support depending on OpenCL* platform hardware capabilities
 - Tradeoff between productivity and portability
- Not all OpenCL* platforms support all SVM features
- OpenCL* 2.0 specification defines a minimum level of required SVM support
 - Other features are optional





- Coarse-grain buffers (Intel 5th Gen Processors w/ HD Graphics 5300)
 - SVM buffers are mapped to either CPU or GPU at any given time
 - Access is controlled by clEnqueueSVMMap/Unmap commands
- Fine-grain buffers (Intel 5th Gen Processors w/ HD Graphics 5500+)
 - SVM buffers can be accessed from either CPU or GPU at any time
 - Use atomics to control access (if CPU & GPU may try to modify the same memory location)
 - Check CL_DEVICE_SVM_FINE_GRAIN_BUFFER for fine-grained buffer SVM support, CL_DEVICE_SVM_ATOMICS is for atomics support
- Fine-grain system memory (Future Intel Processors)
 - CPU & GPU can share anything allocated from the C-runtime 'heap' (i.e. malloc/new)





- Coarse-grain buffers (Intel 5th Gen Processors w/ HD Graphics 5300)
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- Coarse-grain buffers (Intel 5th Gen Processors w/ HD Graphics 5300)
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- Fine-grain buffers (Intel 5th Gen Processors w/ HD Graphics 5500+)
 - SVM buffers can be accessed from both CPU and GPU at any time
 - Can use atomics to avoid 'race' conditions







- Fine-grain system memory (Future Intel Processors)

Refer to **OpenCL* 2.0 Shared Virtual Memory Overview** for more information

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SVM in VTune Amplifier XE Views

Section Se	
Version:	OpenCL C 2.0
Max Compute Units:	24
Max Work Group Size:	256
Local Memory:	64 KB
SVM Capabilities:	Fine-grained buffer with atomics

rouping: Computing Task Purpose / Computing Task (GPU) / Instance											
Computing Task Purpose / Computing Task	Work Size		Computing Task								
(GPU) / Instance	Global	Local	Total Time	Average Time	Instance Count	SIMD Width	SVM Usage Type				
□ Compute			499.664s	0.038s	13,005						
	2097152	256	133.550s	0.157s	849	32					
ReadWriteCopy_NoAlignPartWrite	2097152	256	61.267s	0.072s	850	32	Fine-Grained Buffer				
	2097152	256	47.392s	0.056s	850	32	Fine-Grained Buffer				
	2097152	256	34.491s	0.041s	850	32					
	2097152	256	34.422s	0.020s	1,700	32					
	2097152	256	32.639s	0.038s	850	32	Coarse-Grained Buffer				
	2097152	256	31.976s	0.038s	850	32					

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- Merging kernels reduces memory traffic
 - But mind instruction cache size
- Continue executing kernels until you really need to read the results
 - Use in-order queue and blocking call to clEnqueueMapXXX
- Merging multiple kernels in a pipeline





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- Optimize host API calls
- Reduce Host <> Device memory traffic and bandwidth
- Optimizing memory access
- Maximizing occupancy
- Maximizing computation
- Kernel algorithm optimization





- Accesses to global and constant memory go through
 - L3 cache: GPU-specific, Cache line is 64 byte:
 - LLC: CPU and GPU shared







- Local memory is allocated directly from the L3 cache
 - Divided into 16 banks at a 32-bit granularity





Code Builder Optimizing Memory Access

- **private** memory that is allocated to registers is very efficient to access
- **Private** memory that spills from registers do the same as **Global** memory
 - The performance in this can be very poor
 - There is no locality for ___private memory accesses
 - each work-item accesses a unique cache line for every access to ___private memory





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Global Memory and Constant Memory

- Global, and constant memory bandwidth is determined by the number of the accessed L3 cache lines.
 - If two L3 cache lines are accessed from different work items in the same hardware thread, memory bandwidth is ½ of the memory bandwidth in case when only one L3 cache line is accessed
- Affected by two factors
 - The access pattern function of the work-item global id(s)
 - The work-group dimensions





Access pattern function example: Workgroup = <16,1,1>

x = myArray[get_global_id(0)];



x = myArray[get global id(0) + 1]







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- Highly-banked
 - More important to minimize bank conflicts than to minimize the number of L3 cache lines accesses
 - Local memory accesses have latencies similar to L3\$ hits
 - Using only local memory as a cache is often not productive
 - But, local memory and L3\$ are organized differently







- Each work item in an OpenCL* kernel has access to up to 512 bytes of register space
- Bandwidth to registers is faster than any memory
- Loading and processing blocks of pixels in registers is very efficient!
 - Example: non-separable convolution (filter2D) in OpenCV*



Use available registers (up to 512 bytes) instead of memory, where possible!

Optimization Notice





- Optimize host API calls
- Reduce Host <> Device memory traffic and bandwidth
- Optimizing memory access
- Maximizing occupancy
- Maximizing computation
- Kernel algorithm optimization





- Occupancy is a measure of utilization
- The goal is to keep a sufficient number of work-groups active
 - If one is stalled, another can run on its hardware resource.





- Two primary things to consider:
 - Launch enough work items to keep GPU units busy
 - Compiler may pack up to 32 work items per thread (with SIMD-32).
 - Let the kernel do enough work
 - In short kernels: use short vector data types and compute multiple pixels to better amortize thread launch cost



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- More subtle occupancy issues (when using barriers or local memory):
 - Sub-slices will not run partial workgroups
 - Can be a limiting factor for very large work groups
 - Sub-slices will not run more than 16 (32 on Gen9) work groups
 - Can be a limiting factor for very small work groups
 - Shared Local Memory (SLM) 64KB SLM per sub-slice
 - Can be a limiting factor for kernels that use a lot of local memory
- General advice when using barriers or local memory
 - Experiment with workgroup sizes of 64, 128, or 256
 - Use less than 64 bytes of local memory per work item







- Optimize host API calls
- Reduce Host <> Device memory traffic and bandwidth
- Optimizing memory access
- Maximizing occupancy
- Maximizing computation
- Kernel algorithm optimization



Maximizing Compute Performance

- Prefer float over int, if possible
- Trade accuracy for speed, where appropriate
 - Use native_* and built-ins (or use -cl-fast-relaxed-math)
 - Compiler optimization options that enable optimizations for floating-point arithmetic for the whole OpenCL* program:
 - For example: -cl-mad-enable, -cl-fast-relaxed-math

Used to speedup OpenCV* SURF and HOG!

Optimization Notice



Using OpenCL* 2.0 Workgroup Functions

- The OpenCL* 2.0 standard offers new workgroup built in functions
 - Parallel Primitive popular parallel primitives (scan, reduction)
 - Operations available: add, min, max
 - Allows reductions and scans without exposed local memory or barriers
 - Broadcast Transmit data from one work item to all work items within the workgroup
 - Predicate evaluate a predicate for all work items in a workgroup (any, all)
- Convenient
 - much simpler to use
- Performance efficient
 - Device-specific implementation optimized for the hardware



Using OpenCL* 2.0 Workgroup Functions

- Predicate workgroup functions
 - work_group_reduce_<op> -
 - work_group_scan_exclusive_<op>
 - work_group_scan_inclusive_<op>
 - Operations available: add, min, max

```
__kernel void foo(int *p)
{
...
int prefix_sum_val = work_group_scan_inclusive_add(p[get_local_id(0)]);
...
}
```



prefix_sum_val = [3 4 11 11 15 16 22 25]

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Example: work_group_reduce_add

<pre>local float smem[256]; unsigned int id = get_local_id(0); float smem[id] = sum = input;</pre>	
<pre>if (id < 128) smem[id] = sum = sum + smem[id + 128]; barrier(CLK_LOCAL_MEM_FENCE); if (id < 64) smem[id] = sum = sum + smem[id + 64]; barrier(CLK_LOCAL_MEM_FENCE); if (id < 32) smem[id] = sum = sum + smem[id + 32]; barrier(CLK_LOCAL_MEM_FENCE); if (id < 16) smem[id] = sum = sum + smem[id + 16]; barrier(CLK_LOCAL_MEM_FENCE);</pre>	
if (id < 8) smem[id] = sum = sum + smem[iv + nor, barrier if (id < 8) smem[id] = sum = sum + smem[iv + No exposed local memory or barrier if (id < 4) smem[id] = sum = sum + smem[iv + Code written independent of workor	rs roup size
if (id < 1) smem[id] = sum = sum + smem[i sum = smem[0]; / Intel optimized for Processor Graph	ics

sum = work_group_reduce_add(input);

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- Predicate workgroup functions
 - work_group_all()
 - work_group_any()

```
__kernel void foo (int *in, int *out)
{
    ...
    int gid = get_global_id(0);
    int result = work_group_all(in[gid] < in[gid+1])
    ...
}</pre>
```

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Develop OpenGL^{*} applications with Intel® SDK for **OpenCL**TM Applications

OpenCL* is Great!

- However...
 - Development is not trivial
 - Debugging of parallel processing applications is difficult
 - Optimization of OpenCL* applications is platform-dependent and very challenging



Intel® SDK for OpenCL[™] Applications

The OpenCL* development environment for Intel[®] based platforms

Available for free

Intel® Code Builder for OpenCL[™] API

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- BUILD AND CREATE
 - JumpStart Kit
 - A wizard for creating an OpenCL* project
 - Kernel Development Framework (KDF)
 - Stand alone environment for write, compile and run kernels









Intel® Code Builder for OpenCL[™] API

Comprehensive development environment for the build, debug, and analysis of an OpenCL* applications

- DEBUG
 - Seamless debugging tool for OpenCL* applications
 - OpenCL* API debugger for host side debugging
 - OpenCL* Kernel Debugger for device side debugging

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Optimization Notice





Intel® Code Builder for OpenCL[™] API

Comprehensive development environment for the build, debug, and analysis of an OpenCL* applications

- ANALYZE
 - Easy and simple performance debugging tool
 - Collect performance data from both the host side and the kernel side

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Intel® Code Builder for OpenCL[™] API

Comprehensive development environment for the build, debug, and analysis of an OpenCL* applications

- Integration
 - A single framework for all the functionality that the developer needs
 - Smooth path between all components
 - IDE native integration



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Debug

Build and create

Create new OpenCL* Project

- Create OpenCL* project with Jump-Start wizard
 - Very simple wizard for creating new OpenCL* project
 - Intended for developers that write an OpenCL* application from scratch
 - Plug in for Visual Studio*



Create new OpenCL* Project

- In a few clicks you can generate:
 - An empty project ready for you to implement host and kernel code
 - Full host + kernel code project ready for build

	New Project		? ×		
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Optimization Notice

Kernel Development Framework (KDF)

- Standalone environment for kernel development
- Syntax checking and auto-completion for OpenCL* C language
- Offline compilation and binary generation of OpenCL* kernels
- Compilation error reports

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Kernel Development Framework

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τe α	50	unit dettystride = get_global size(0);	19	0xc0	mac	h (8 M0)	null<1>:d	r51.0<8;8,1>:d	r2.0
7	57	unit dstindex = get_global_id() * dstistride + get_global_id(0);	20	0xc8	mov	(8 M0)	r55.0<1>:d	acc0.0<8;8,1>:d	
ě.	58	unit srctstride = dstystride + 2 ;	21	0xd8	add	(16 M0)	r59.0<1>:d	r53.0<8;8,1>:d	r57.(
ŏ.	59	$\operatorname{unc} \operatorname{srcindex} = \operatorname{get} \operatorname{grobal} \operatorname{Id}(1) = \operatorname{srcystride} + \operatorname{get} \operatorname{grobal} \operatorname{Id}(0) + 1;$	22	0xe0	add	(16 M0)	r63.0<1>:d	r59.0<8;8,1>:d	1:d
-	60		23	0xe8	add	(16 M0)	r68.0<1>:d	r63.0<8;8,1>:d	r67.(
	61	uint a; uintib b; uint c;		0xf0	shl	(16 M0)	r70.0<1>:ud	r63.0<8;8,1>:ud	0x4:1
	62	uint d; uint16 e; uint +;	25	0xf8	shl	(16 M0)	r81.0<1>:ud	r68.0<8;8,1>:ud	0x4:i
	63	uint g; uint16 h; uint 1;	26	0x100	add	(16 M0)	r85.0<1>:ud	r70.0<8;8,1>:ud	0xC:L
	64			0x108	add	(16 M0)	r79.0<1>:ud	r70.0<8;8,1>:ud	0xFFI
	65	// Read data in	28	18	add	(16 M0)	r91.0<1>:ud	r81.0<8;8,1>:ud	0xC:i
	66	<pre>a = ((global uchar*)(pSrcImage+srcIndex))[-1]; b = convert</pre>	29	0XL	add	(16 M0)	r95.0<1>:d	r85.0<8:8.1>:d	-12:0
	67	<pre>srcIndex += srcYStride;</pre>	30	0x130	add	(16 M0)	r87.0<1>:ud	r81.0<8:8.1>:ud	ØxFFI
	68	<pre>d = ((global uchar*)(pSrcImage+srcIndex))[-1]; e = coert_uint16(pSrcIma</pre>	31	0x140	add	(16 M0)	r103.0<1>:d	r91.0<8:8.1>:d	-12:0
	69	<pre>srcIndex += srcYStride;</pre>	32	0x150	add	(16 M0)	r74.0<1>:d	r68.0<8:8.1>:d	r67.6
	70	<pre>g = ((global uchar*)(pSrcImage+srcIndex))[-1]; h = convert_uint16(pSrcIma</pre>	33	0x158	sen	d (16 M0)	r33:uw	r95	0xC
	71		34	0x168	add	(16 M9)	r93.0<1>:ud	r81.0<8:8.1>:ud	0x10
	72	uint16 xVal, yVal;	35	0x170	sen sen	d (16 M9)	r113:uw	r87	0xA
	73		36	0x180	sen	d (16 M9)	r105:uw	r79	0xA
	74	xVal = (uint16)(a, b.s0123, b.s456789ab, b.scde)t16)(b.s123, b.		8v100	bbe	(16/M0)	n93_0/15+ud	n70 0/818 1510d	0x10
	75	2*(uint16)(d, e.s0123, e.s456789ab, e.scde) - 2*(u 16)(e.s123, e.	2.0	0x190	Son	(16 M0)	n25:00	n102	0XI0
	76	(uint16)(g, h.s0123, h.s456789ab, h.scde) - (uint 16, s123, h.	20	UNI	chl	(16 MQ)	n20.0/12:ud	p74 0/9+9 15+ud	0x4.1
	77		33	-av1b0	500	(16 M0)	nE:0017.00	n02	0x4.0
	78	yVal = (uint16)(a, b.s0123, b.s456789ab, b.scde) + 2*b + (uint16)(b.s123, t	41	Ox100	Sen	d (16 M0)	n111.000	195	0xA
	79	(uint16)(g, h.s0123, h.s456789ab, h.scde) - 2*h - (uint16)(h.s123, h	41	Ox1C0	sen	u (16 M0)	rilliuw r00.0415.uud	n00 04040 1544	OXA
	80		42	01140	auu	(16 10)	r99.0(1):uu	r89.0(8;8,1):uu	OxC:I
	81	// Write data out	43	0x108	add	(10 M0)	r97.0(1):ud	1.89.0(8;8,1):Ud	0xFFI
	82	<pre>pDstImage[dstIndex] = convert uchar16(min((float16)255.0f, sort(convert flc.)</pre>	44	0x1e8	add	(10 M0)	r101.0<1>:ud	1'89.0(8;8,1):Ud	0110
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Gen assembly <> OpenCL*-C Line mapping

Optimization Notice

Code Builder

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Kernel Development Framework

- Run and review the results
 - Assign variables to the kernel and check its correctness
 - Show the input and output values
- Capture kernel session from exiting OpenCL* application
 - Store the kernels code with its inputs (buffer or images)

- Coming soon:
 - Generate host code from session
 - Validate kernel outputs versus a reference

Optimization Notice



Capture & Reply Kernel Sessions





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80

Capture & Reply Kernel Sessions

- Very useful when kernel inputs are not available
 - Created in run-time
 - Output of a previous kernel
- Very useful when the application requires user interaction to execute the kernel
- Eliminates the need to run the application for any kernel change

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- Sobel Kernel
 - Edge detection algorithm
 - Discrete differentiation operator, computing an approximation of the gradient of the image intensity function
 - https://en.wikipedia.org/wiki/Sobel_operator









- Generate session from CyberLink Power Director* A High Performance Video Editing suite



Optimization Notice





- Seamless debugging of OpenCL* API calls, objects, and queues
- Enables monitoring and understanding the OpenCL* environment of an application execution
- OpenCL* API call tracing
- Images and memory objects view
- Extension to the Visual Studio* debugger



Objects Tree View Explore all OpenCL* objects in memory and their properties

Commands Queue View Examine commands queue status and their commands' state

Date View Image View Show the content of OpenCL* Show the visualized content × SobelFilterApp (Debugging) - Microsoft Visual Studio memory objects (buffers + images) FILE EDIT VIEW PROJECT BUILD DEBUG TEAM SQL TOOLS of OpenCL* image objects ય છે. -G - O Continue - Aut E 🔿 🚽 😼 🗁 🛐 🔮 🚛 🗔 🝦 OpenCL Platform Intel(R) OpenCL OpenCL Device OPU: Intel(K) HD Graphic * Target Are Process: [4196] SobelFilterApp.exe 🔹 💽 Suspend 👻 🎦 Thread: [8264] Main Thread 🔻 🛒 🖂 Stack Frame: wmain SobelFilter.cpp • # × main.cpp + × SobelFilter.cl ice [1] 💵 Sort By 🔹 🧠 Show Objects 🔹 (Global Scope) HAR * argv[1) 68 - Representation Platform [1] (Intel(R) OpenCL) 2↓ 🖾 69 // retrieve perf. counter frequency Max Constant Buffer Size (I 131072 70 app->PerformanceReport(); 71 Max Constant Arguments | 480 CommandQueue [1] (In Order) 72 // cleanup all resources Other Information - Program [1] (Built) app->Cleanup(); Vendor ID 32002 🛓 🐻 Kernel [1] (SobelFilter 74 Device Type CL DEVICE TYPE CPU Sam. 75 if(false == res) Single Precision fp al Input 76 100 % -CL FP DENORM Outout [0] CL_FP_INF_NAN A Mack [1] Data View ▼ ↓ × Image View - A [2] CL FP ROUND TO NEAREST - 📰 Image [3] Memory Object: Image [1] History: 42: clEngueueWriteImage Save As.. History; Image: Image [1] -📰 Image [4] **Execution Capabilities** CL EXEC KERNEL [0] - 🔳 Buffer [2] 0.89,0.54,0.49,1.00 (0.87,0.54,0.52,1.00) (0.87,0.53,0.50,1.00) (0.89,0.54,0.47,1.0 1 [1] CL_EXEC_NATIVE_KERNEL Context [2] (0.89,0.54,0.49,1.00) (0.89,0.54,0.49,1.00) (0.87,0.54,0.52,1.00) (0.87,0.53,0.50,1.00) (0.89,0.54,0.47,1.0 Global Memory Cache Typ CL READ WRITE CACHE Device [2] (GPU) Local Memory Type CL GLOBAL (0.89,0.54,0.49,1.00) (0.89,0.54,0.49,1.00) (0.87,0.54,0.52,1.00) (0.87,0.53,0.50,1.00) (0.89,0.54,0.47,1.0 3 - II CommandQueue [2] (In Order) Address Bits (Bytes) (0.89.0.54.0.49.1.00) (0.89.0.54.0.49.1.00) (0.87.0.54.0.52.1.00) (0.87.0.53.0.50.1.00) (0.89.0.54.0.47.1.0 4 Event [2] (ndrange_kernel) Memory Base Address Alig 1024 CommandQueue [3] (In Order) (0.89,0.54,0.49,1.00) (0.89,0.54,0.49,1.00) (0.87,0.54,0.52,1.00) (0.87,0.53,0.50,1.00) (0.89,0.54,0.47,1.0 Min Data Type Align Size (I 128 - 🕞 Event [1] (write image) (0.89,0.55,0.48,1.00) (0.89,0.55,0.48,1.00) (0.89,0.51,0.44,1.00) (0.87,0.51,0.44,1.00) (0.89,0.53,0.47,1.0 6 Device Extensions B- Program [2] (Built) (0.89.0.53.0.47.1.00) (0.89.0.53.0.47.1.00) (0.88.0.55.0.45.1.00) (0.88.0.52.0.45.1.00) (0.88.0.53.0.49.1.0 7 [0] cl_khr_fp64 - Kernel [2] (SobelFilter) (0.87.0.52.0.47.1.00) (0.87.0.52.0.47.1.00) (0.89.0.51.0.42.1.00) (0.87.0.52.0.45.1.00) (0.89.0.51.0.47.1.0 [1] cl khr icd 8 🔊 Sam [2] cl_khr_global_int32_base_atom Code Builder Analysis Inp... Objects Tree Solution Explorer Class View [3] cl_khr_global_int32_extended_a Trace View Command Queue - 0 × [4] cl_khr_local_int32_base_atomic 🔬 Save... 👻 Load Session... 👩 Success 😣 Errors 🛛 API Display Mode 🗸 Filter 🔜 Save As... 🧠 Seperate Queues Sort By Time: Ascending [5] cl khr local int32 extended at cl_khr_byte_addressable_store CommandQueue [1] (CPU, In Order) API Return Value Error Code Time [6] [7] cl_intel_printf CL_SUCCESS CL_SUCCESS 15:58:30:235 63 clReleaseContext(Context [2]) CL SUCCESS CL_SUCCESS 15:58:30:234 [8] cl ext device fission 62 clReleaseContext(Context [1]) Submitted Running Completed [9] cl_intel_exec_by_local_thread 61 clReleaseCommandOueue(CommandO... CL SUCCESS CL SUCCESS 15:58:30:234 [10] cl khr al sharing 60 clReleaseCommandOueue(CommandO... CL SUCCESS CL SUCCESS 15:58:30:232 [11] cl_intel_dx9_media_sharing READ IMAGE(2) COI1 59 clReleaseProgram(Program [2]) CL_SUCCESS 15:58:30:232 WRITE IMAGE(3) CO [12] cl_khr_dx9_media_sharing 58 clReleaseProgram(Program [1]) CL SUCCESS CL SUCCESS 15:58:30:231 NDRANGE KERNEL (4 57 clReleaseKernel(Kernel [2] (SobelFilter)) CL_SUCCESS CL SUCCESS 15:58:30:216 Vendor ID READ IMAGE(5) CO[3] Not Available 56 clReleaseKernel(Kernel [1] (SobelFilter)) CL SUCCESS CL SUCCES 15:58:30:213 Call Stack Breakpoints Output Trace View Autos Locals Threads Modules Watch 1 • 4 × Problems view 🔞 0 Errors 🛕 2 Warnings # Decription 🛕 2 Context [2] was released before CommandQueue [3] (In Order) with CommandQueue [3] (In Order) having Reference Count = 1. **Trace View Properties View** Trace application's OpenCL* API View the properties of the calls and their return values selected OpenCL* objects

Problems View Look for hints for potential error or warnings during execution

Host Level Debugging

- Image view
 - Show the visualized content of OpenCL* Image objects when hitting the break point
 - Option to see the image content in different stages of the program
 - Channel filter
- Data view
 - Show the content of OpenCL* memory objects (buffers + images)



Optimization Notice



- Object tree view
 - Hierarchical view of all OpenCL* objects in memory
 - Filter objects by type
- Properties view
 - View the properties of the selected OpenCL* objects

Objects Tree	- ₽ ×	
🔰 Sort By 🝷 ዀ Show Objects 🝷		1
Sort By • Show Objects • Platform [1] (Intel(R) OpenCl Context [1] Context [1] CommandQueu Program [1] (Bu Kernel [1] (S Mage [3] Sampler [2] Context [2] CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQueu CommandQue	L) Properties View Image [3] A Basic Information Reference Count Key	
	Channel Order Not Available	
L		



- Problems view
 - Look for hints for potential error or warnings during execution
 - Filter for errors/warning

Pro	bler	ns view 🝷 📮 🗙
8) O E	rrors 🕂 3 Warnings
-	#	Decription
▲	1	Kernel [2] (SobelFilter)'s argument number 1 is not initialized yet
Δ	2	Kernel [2] (SobelFilter)'s argument number 2 is not initialized yet
Δ	3	Kernel [2] (SobelFilter)'s argument number 3 is not initialized yet







- Trace view
 - Show for any executed OpenCL* API:
 - Name and arguments
 - Error code
 - Return value
 - Execution time
 - Filter by errors/success

Tra	ce View			ب	×
R	Save 👻 Load Session 🛛 🐼 Success 🐼 Errors	API Display Mode 👻		Filter:	
	API	Return Value	Error Code 🛛	Time	*
25	clCreateImage(Context [1], CL_MEM_READ_ONLY	lmage [3]	CL_SUCCESS	10:03:40:720	
24	clCreateSampler(Context [2], CL_FALSE, CL_ADDR	Sampler [1]	CL_SUCCESS	10:03:40:712	
23	clCreateImage(Context [2], CL_MEM_WRITE_ONL	Image [2]	CL_SUCCESS	10:03:40:610	
22	clCreatelmage(Context [2], CL_MEM_READ_ONLY	lmage [1]	CL_SUCCESS	10:03:40:481	
21	clGetDeviceInfo(Device [2] (CPU), CL_DEVICE_ME	CL_SUCCESS	CL_SUCCESS	10:03:37:856	-





- Commands queue view
 - Examine commands queue status and their commands' state
 - Help understand the commands flow thru the various queues during the application

Command Queue		→ ↓ ×
🍋 Unify Queues		Sort By Time: Ascending
CommandQueue [1] (CPU, In Order)		¥
Submitted	Running	Completed
NDRANGE_KERNEL(1)	WRITE_IMAGE(0)	

- Enables source and assembly level debugging on GPU
- Provide all the conveniences of the modern debugger
 - Step-in, break and continue, show variables, switch between threads, etc.
- Enhanced for the specifics of OpenCL
 - Ability to view the content of vector variables like float4, uchar16 etc.
- Remote debugging only (host vs. target)
- GDB based
- Microsoft Visual Studio* 2015 integration
- Supported on Gen9 and above (Beta version) on Windows





Optimization Notice



Disassembly				- ų	×
Address: SobelFilter					•
Viewing Options					
0x00000000000920e0	(W)	mul	(1 M0)	r18.0<1>:uw	
0x0000000000920f0	(W)	add	(1 M0)	a0.0<1>:uw	
0x0000000000092100	(W)	mov	(1 M0)	r14.0<1>:d	
0x000000000092110	(W)	mul	(1 M0)	r12.0<1>:q	
0x0000000000092120		mov	(8 M0)	r13.0<1>:d	
0x000000000092130		mov	(8 M0)	r6.0<1>:q	
0x000000000092140		add	(8 M0)	r15.0<1>:q	
0x000000000092150	(W)	mov	(1 M0)	r17.0<1>:q	
0x000000000092160		add	(8 M0)	r19.0<1>:q	
0x000000000092170		mov	(8 M0)	r8.0<1>:d	
0x000000000092180		sends	(8 M0)	null:ud	
© 0x000000000092190	(W)	mov	(1 M0)	r5.14<1>:w	
0x00000000000921a0	(W)	cmp	(8 M0)	[(eq)f0.0] null<1	E
0x00000000000921b0	(W)	mov	(1 M0)	r9.0<1>:w	
0x0000000000921c0	(W&f0.0)	sel	(1 M0)	r10.0<2>:b	
0x00000000000921d0	(W)	mov	(1 M0)	r11.0<1>:d	
0x00000000000921e0	(W)	add	(1 M0)	r14.0<1>:d	
0x00000000000921f0	(W)	mul	(1 M0)	r13.0<1>:uw	
0x000000000092200	(W)	add	(1 M0)	a0.0<1>:uw	
0x000000000092210	(W)	mov	(1 M0)	r6.0<1>:d	
0x000000000092220	(W)	mul	(1 M0)	r7.0<1>:q	
0x000000000092230	30.59	mov	(8 M0)	r12.0<1>:d	w
4			- 1	•	
Disassembly Diagnostic To	ools				

Optimization Notice



Comman	d Window	Watch 1 🕫 🗙		Ŧ
Name		Value	Туре	-
Þ 🥥 S	r10.v8_int32	[8]	v8i32	
Þ 🖌 S	r25.v8_int32	[8]	v8i32	
Þ 🥥 f!	Sobel@8	[8]	float4 [8]	
Þ 🥥 S	r23.v8_int32	[8]	v8i32	
DOS	r6.v8_int32	[8]	v8i32	
4 🤗 X	@8	[8]	int [8]	
	[0]	0	int	
	[1]	1	int	
	[2]	0	int	
	[3]	1	int	
	[4]	0	int	
	[5]	0	int	
	[6]	0	int	
9	[7]	0	int	
K 🖸 Y	@8	[8]	int [8]	
13 0	[0]	0	int	
	[1]	0	int	
	[2]	1	int	
	[3]	1	int	
	[4]	0	int	
0	[5]	0	int	
0	[6]	0	int	
	[7]	0	int	
				-

Name	Value	Туре
_ocl_dbg_gid0	2	unsigned long
_ocl_dbg_gid1	2	unsigned long
_ocl_dbg_gid2	0	unsigned long
_ocl_dbg_lid0	0	unsigned long
_ocl_dbg_lid1	0	unsigned long
_ocl_dbg_lid2	0	unsigned long
_ocl_dbg_grid0	1	unsigned long
_ocl_dbg_grid1	1	unsigned long
_ocl_dbg_grid2	0	unsigned long
	2	int
Y	2	int
PixelCoords	[2]	int2
🕨 🤗 fSobel	[4]	float4
Sam	1	opencl_sampler_t
Input	0x20100000000000	struct opencl_image2d_t *
🕨 🥔 Mask	0xa28c062000	int *

Optimization Notice

Kernel Level Debugging on the GPU Step by Step source level debugging of the GPU EU

threads Quick Launch (Ctrl+Q) Р _ 6 X Microsoft Visual Studio Switch between Project Build Debug Team Tools Test Code-Builder Analyze Window Help Sign in 🏼 🎴 0 - 0 13 - 🖆 🐸 🥙 - C - Debug - x64 🕨 Continue 🔹 🏓 🚆 📆 🗁 🚼 🕖 🔮 🐺 🗔 🚊 Select Kernel SobelFilter - ▶ 🖂 📚 📲 🗉 = 🌢 🔞 → 🔹 😨 🚼 裕 🚆 岩 昭 🗐 🗵 独 📕 🌾 🦓 神 神 二章 🧐 No Application Insights Events - 🖕 **GPU EU threads** Process: [N/A] Intel GPU Stub - F Lifecycle Events - Thread: [1073741824] - 🔻 🐖 🚧 Stack Frame: SobelFilter · . earch - X Search Call Stack 🛛 🔻 - 🛒 🚧 Group by: Process ID - Columns - 🗉 🖬 💣 🗗 📗 🕨 ID Managed ID Category Name Location Priority 1610612736 0 2 Worker Thread EMPTY CODE Normal 1073742336 (? Worker Thread ✓ !SobelFilter Normal 1073742144 0 7 Worker Thread ✓ !SobelFilter Normal 1073741888 0 2 Worker Thread ✓ !SobelFilter Normal 1073741824 0 7 Worker Thread ✓ !SobelFilter Norma Assembly level Address: SobelFilte debugging Viewing Options _kernel void SobelFilter(sampler_t Sam, sends (8 M0) null:ud r53 0x40 9x4068 __read_only image2d_t Input, write only image2d t Output, send (8 M0) r10:d r49:ug 0xC 0x41401F 0xC global int* Mask) send (8M8) r11:d r53:ug 0x41401FF exeeeeeeeeeeeeeeeee (8M8) c53:00 0xC 8x41481FF r13.0<1>:d r10.0<8:8.1>:d mov (8M8) int X = get global id(0); int Y = get_global_id(1); (8M8) r14 0(1):d r11.0<8;8,1>:d sends (8140) null:ud r51 0x80 0x40685F r51:uq (81M0) r21:d 0×C 0v42405FF // Read image coordinates (8100) r6.0<1>:f r21.0<8;8,1>:d mov int2 PixelCoords = {X,Y}; ~88888988888 (8|M0) r7.0<1>:f r22.0<8;8,1>:d float4 fSobel = read_imagef(Input, Sam, PixelCoords); x0000000000090320 mov (1 M0) r4.1<1>:ud 0x0:uw Step by step 000090330 mov (1 | M0) r4.0<1>:ud 0x1:uw if (Mask[X] == 1) 0090340 mov (1 M0) r35.2<1>:ud 0x0:ud kernel source-(8 M0) r8.0<1>:f r6.0<8;8,1>:* float4 p[3][3]; mov (8 M0) r9.0<1>:f r7.0<8;8,1>:f for (int horizontal = 0; horizontal < 3; ++horizontal) {</pre> 00090370 add (1 M0) a0.0<1>:ud r4.0<0:1.0>:ud 0x2488000:ud for (int vertical = 0; vertical < 3; ++vertical) { sh1 (11M8) r5.7(1):ud r4.1<0:1.0>:ud By8:ud **Global memory** level debugger int2 Coords = {X+horizontal-1, Y+vertical-1}: (1 | M0) p[horizontal][vertical] = read_imagef(Input, Sam, Coords); add a0.0<1>:ud a0.0<0:1.0>:ud r5.7<0:1.0>:u (81M8) c10.f c35 **r**8 a0.0 sends (8|M0) null:f c55 r10 9x19C 0x40689E view r49:ug (8|M0) r14:d 0×C 0v41401EE mov (8 M0) r15.0<1>:q r14.0<8;8,1>:d float4 SobelH = p[2][0] - p[0][0] + 2 * (p[2][1] - p[0][1]) + p[2][2] - p[0][2] float4 SobelV = p[0][0] - p[0][2] + 2 * (p[1][0] - p[1][2]) + p[2][0] - p[2][2]; Watch ' Value Type Nam Type ddress: 0x0000001630e1b000 - 🖒 Columns: Auto _ocl_dbg_gid0 unsigne _ocl_dbg_gid1 unsigne IO1 _ocl_dbg_gid2 unsigne (11) int32_t Local and Global int32 t ocl dbg lid unsigne int32 t ocl dbg lid! unsigne (3) int32_t variables view _ocl_dbg_lid2 unsigne [4] _ocl_dbg_grid(unsigne (5) int32_t int32_t _ocl_dbg_grid1 unsigne @ [6] 2732 Inspect int32_t _ocl_dbg_grid2 unsigne (7) 0) int [8] **GPU** register int [8] 01 int Y@8 PixelConrds v8i32 int2 \$r25,v8 int32 [8] b @ (Sobel float4 FSobel@8 float4 [8] values Sam opencl Input 0v20100000000000 struct o A Mask 0x1630e1b000 int* prv1 Call Stack, Breakpoints, Excention Settions, Command Window, Immediate Window, Output Lutos Locals

Optimization Notice

Code Builder



Code Builder ANALYZE Performance Analysis with Code Builder

- 2 ways for performance analysis with the Code Builder
 - Kernel level analysis only with the Kernel Development Framework
 - Full application analysis (host + kernels)



Code Builder – kernel Analysis with KDF

- Kernel Development Framework enable a standalone environment for performance analysis of kernels
 - Enables What-if analysis
 - Provides a lot of performance data:
 - Throughput
 - Memory bandwidth
 - GPU utilization
 - Occupancy
 - Latency for memory operation

Optimization Notice





- Generate session from CyberLink Power Director* A High Performance Video Editing suite



Optimization Notice



- Optimization of Sobel Kernel
 - Uchar -> Uchar16
 - Int -> float





(intel)

Optimization Notice

Code Builder - Full Application Analysis

- Guided performance debugging and source level analysis capabilities
 - a "wizard-like" profiling tool with runtime hints and drill down analysis (host to kernel)
 - Command line tool
 - Fully integrated to Visual Studio*



Optimization Notice





Target application: Optical Flow (OpenCV* implementation)

Given a set of points in an image > find those same points in another image



Optimization Notice



DEMO – Full Application Analysis with Code Builder

Target application: Optical Flow (OpenCV* implementation)

Given a set of points in an image > find those same points in another image

- Can be used to:
 - Find an object from one image in another
 - Determine how an object/camera moved
 - Resolve depth from a single camera.
 - More..
- Use a lot of OpenCL* kernels



Optimization Notice







Intel® VTune Amplifier XE

Code Builder



VTune analysis of Microsoft* HTML5 Fish Bowl application http://ie.microsoft.com/testdrive/performance/fishbowl/

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intel

Code Builder OpenCL™ Command Queue View







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SVM Usage Info

⊗ GPU OpenCL Info	
Version:	OpenCL C 2.0
Max Compute Units:	24
Max Work Group Size:	256
Local Memory:	64 KB
SVM Capabilities:	Fine-grained buffer with atomics

Grouping: Computing Task Purpose / Computing Task	(GPU) / Insta	ince						
Computing Task Purpose / Computing Task	Work Size		Computing Task					1
(GPU) / Instance	Global	Local	Total Time v	Average Time	Instance Count	SIMD Width	SVM Usage Type	L
∃ Compute			499.664s	0.038s	13,005			L
	2097152	256	133.550s	0.157s	849	3		L
ReadWriteCopy_NoAlignPartWrite	2097152	256	61.267s	0.072s	850	3	Fine-Grained Buffer	L
	2097152	256	47.392s	0.056s	850	3	Fine-Grained Buffer	Γ
	2097152	256	34.491s	0.041s	850	3		K
⊞ ReadOnly	2097152	256	34.422s	0.020s	1,700	3		I
	2097152	256	32.639s	0.038s	850	3	Coarse-Grained Buffer	I
	2097152	256	31.976s	0.038s	850	3		L



Gaussian Blur

Naïve implementation

- Uses Sampler
- Process one pixel per a work-item





Gaussian Blur



```
const sampler t samplerA = CLK FILTER NEAREST ;
kernel void gaussian blur naive(read only image2d t src,
                                 __global float* table,
                                 const int blur radius,
                                 write only image2d t dst)
   float4 dst_val = { 0, 0, 0, 0}, src_val = { 0, 0, 0, 0};
   int i, k, h, w;
   int x = get_global_id(0);
   int y = get global id(1);
   int table width = blur radius*2 + 1;
   for (i = 0; i 
       w = i - blur radius;
       for (k = 0; k < table_width; ++k)</pre>
           h = k - blur_radius;
           src val = read imagef(src, samplerA, (int2)(x + w, y + h));
           dst val += src val * table[i*table width + k];
   write imagef(dst, (int2)(x, y), dst val);
```

* Code source by Intel

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What Can We Learn from VTune ?



* Code source by Intel

EUStalled ~ $0.2 \Rightarrow$ EUs are waiting 20% of the time

Gaussian Blur: Can We Do Faster ?

Use memory buffers instead of images

Memory buffers are faster to access then Sampler

- Take advantage of Gaussian Blur's separability property
- Two kernels (instead of one):
 - Horizontal pass
 - Vertical pass







Code given here just for a reference. It is not recommended to use it after the Webinar

Gaussian Blur: Two Passes

kernel void gaussian_blur_hor_1(__global uchar4* src,

float4 _unpack_uchar4(uchar4 src)
{
 private uchar4 temp = src;
 float4 res;
 res.x = (float)temp.x;
 res.y = (float)temp.y;
 res.z = (float)temp.z;
 res.w = (float)temp.w;
 return res;
}

uchar4 _pack_float4(float4 src)
{
 uchar4 res;
 res.x = (uchar)src.x;
 res.y = (uchar)src.y;
 res.z = (uchar)src.z;
 res.w = (uchar)src.w;
 return res;
}

```
global float* table.
                            const int blur radius,
                            global uchar4* dst)
float4 dst_val = { 0, 0, 0, 0}, src_val = { 0, 0, 0, 0};
int x = get global id(0);
int y = get global id(1);
int image_width = get_global_size(0);
for (int k = 0; k < blur radius*2 + 1; ++k)
    int w = x + k - blur radius:
   if (w \ge 0 \& w < image width)
        src val = unpack uchar4(src[image width*y + w]);
    else if (w < 0)
        src val = unpack uchar4(src[image width*y]);
    else if (w >= image width)
        src val = unpack uchar4(src[image width*y + image width-1]);
   float4 mult = (float4)table[k];
   dst val += src val * mult;
dst[v*image width + x] = pack float4(dst val);
```

__kernel void gaussian_blur_vert_1(__global uchar4* src, global float* table. const int blur radius. global uchar4* dst) float4 dst val = { 0, 0, 0, 0 }, src val = { 0, 0, 0, 0 }; int x = get global id(0);int y = get global id(1);int image width = get global size(0); int image_height = get_global_size(1); for (int k = 0; k < blur_radius*2 + 1; ++k)</pre> int w = v + k - blur radius: if ($w \ge 0$ && w < image height) src val = unpack uchar4(src[image width*w + x]); else if (w < 0)src val = unpack uchar4(src[x]);else if (w >= image_height) src_val = _unpack_uchar4(src[(image_width)*(image_height-1) + x]); float4 mult = (float4)table[k]; dst val += src val * mult: dst[y*image width + x] = pack float4(dst val);

* Code source by Intel

Two passes give 21 ms of device time instead of 30 ms! EUActive increased from 0.8 to 0.9

Gaussian Blur: Two Passes



EU <-> L3 memory bandwidth is far from its peak value (~37 Gb/s vs. 150 Gb/s)

Gaussian Blur Optimization Steps

Kernel	Time, ms	EUActive	EUStalled	EUIdle	L3 Reads, Gb/s	L3 Writes, Gb/s	An increase of EUActive and L bandwidth
Naïve	30	0.78	0.21	0.014	N/A	N/A	
Hor Pass Simple 1 pixel per work-item	9.9	0.89	0.10	0.019	30	1.5	
Vert Pass Simple 1 pixel per work-item	11	0.85	0.091	0.059	20	1.5	
Total*	21.8						
Hor Pass 4 pixels per work-item	5.6	0.89	0.094	0.015	54	3.0	
Vert Pass 4 pixels per work-item	5.8	0.68	0.68	0.006	25	2.9	
Total*	13.5						
Hor Pass 8 pixels per work-item	4.6	0.93	0.064	0.006	68	7.3	
Vert Pass 8 pixels per work-item	4.9	0.96	0.038	0.003	53	6.7	
Total*	10.8						

Sum of kernels duration + time between the kernels

Performance data where collected on Intel® 4th Generation Intel® Core™ Processor with Intel® HD Graphics 5000



