ENPOWER: An OpenCL Approach for Energy Proportional Computing With Heterogeneous and Reconfigurable Processors

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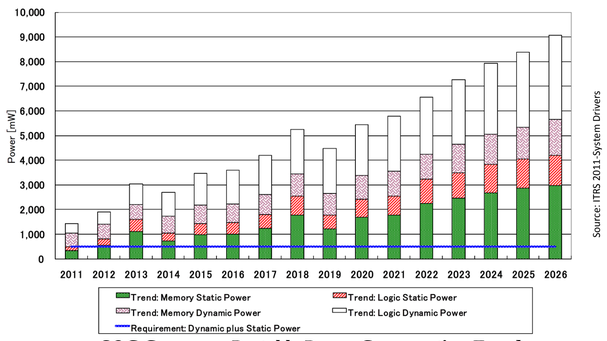
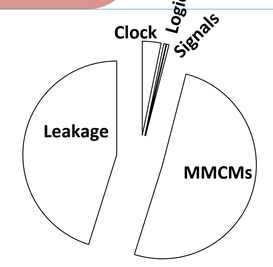
1- Abstract

- Energy proportional computing applied to hybrid FPGA-ARM chip
- This research proposes the concept of energy proportional computing includes scalability of a power triplet formed by
  - Voltage,
  - Frequency and
  - Logic (e.g. capacitance)
- Applications in this design paradigm are written in an extended OpenCL

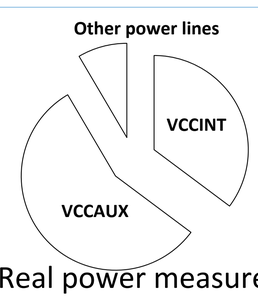
2- Motivations



SOC Consumer Portable Power Consumption Trends

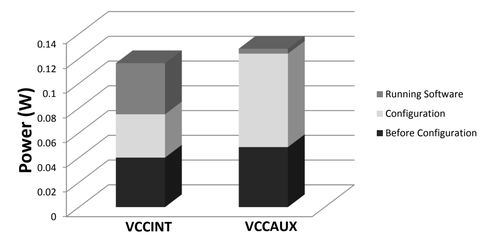


Xilinx XPower Analyzer



Real power measurement on ZC702

A simple motivation example is considered in this subsection. The example consists of a MicroBlaze soft processor core configured in the PL and the ARM processor available in the PS. The MicroBlaze runs a 32 x 32 floating point matrix multiplication.



MicroBlaze power consumption

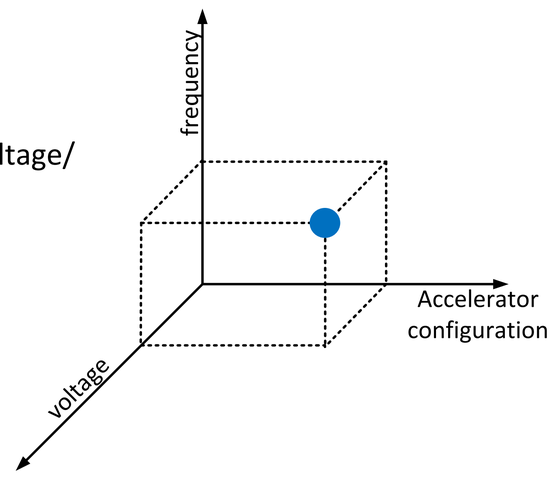
3-Goals

- Propose a new design paradigm in order to expose the concept of energy proportional computing to the application software
- Considering the logic and power scalability in a variation-aware closed-loop configuration
- Using a software centric approach based on OpenCL for describing applications
- Using a processor-centric platform such as Xilinx All Programmable SoCs to implement applications

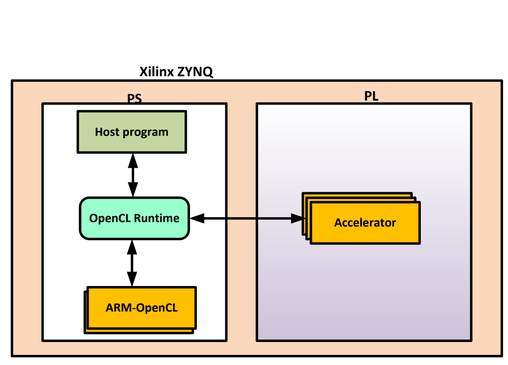
Role of OpenCL runtime

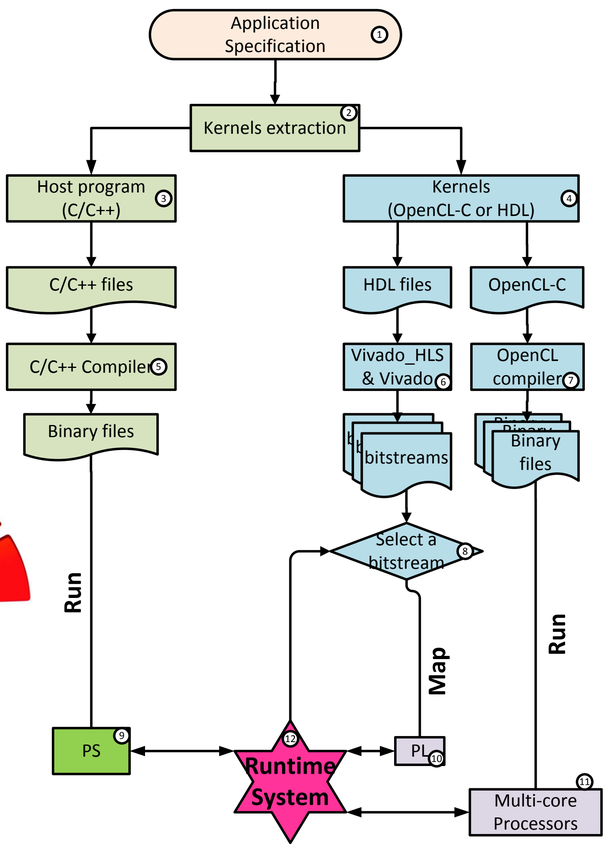
Choosing the best configuration and voltage/ frequency at run time.

- scheduling
- mapping algorithm.



4-Contributions





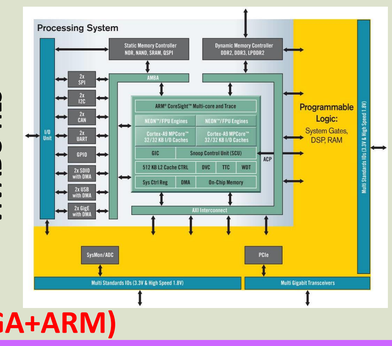
System-level issues

- Power modelling
- Energy modelling
- Power gating
- Power scaling
- Clock gating
- Frequency scaling
- Logic scaling

OpenCL

5-Framework

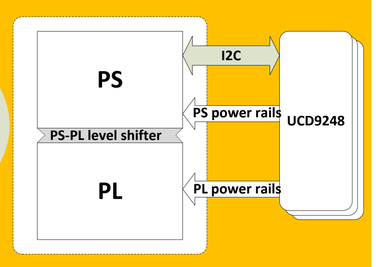
ZYNQ all Programmable SOC

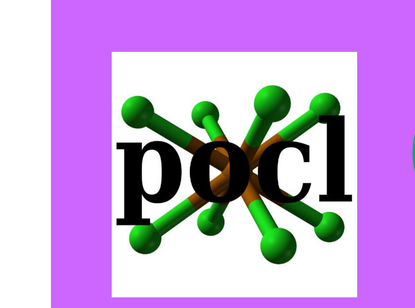


VIVADO & VIVADO-HLS

(FPGA+ARM)

System-Level Power Control





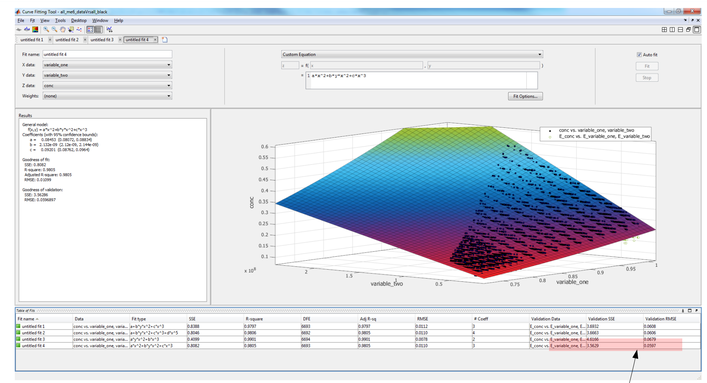
6-Power & Energy Modelling (prerequisite research)

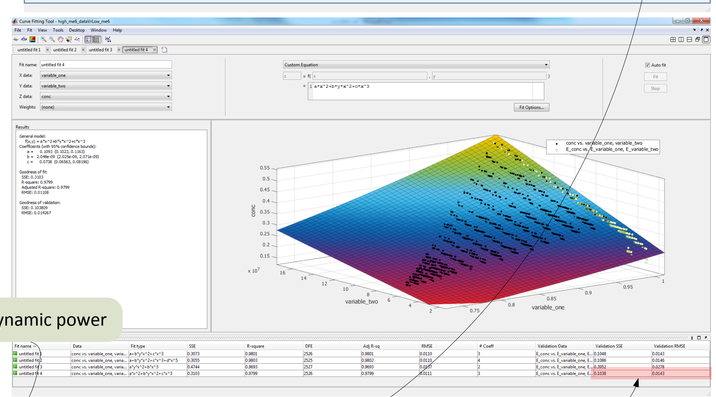
High-Level Models should be:

- Covers PL, PS and memories
- Simple
- Compositional
- Descriptive

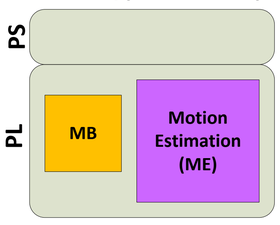
Specially the PL High-Level Models should:

- Describes different thread hardware and cores
- Describes different accelerator modes
  - Idle
  - Data transfer
  - Active
  - Computational





ZYNQ (FPGA+ARM)



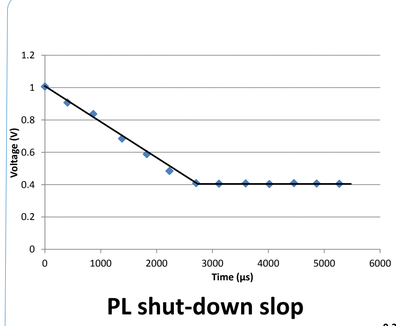
ME dynamic power

Dynamic power caused by measurement modules with own frequency

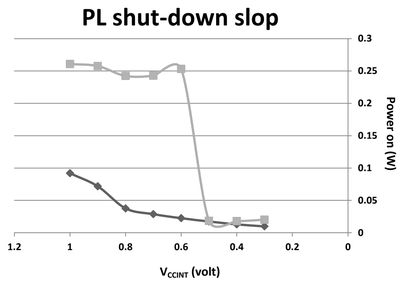
Static power

$$\text{PL Power for ME} = a*V^2 + b*f*V^2 + c*V^3$$

7-Power Gating (prerequisite research)

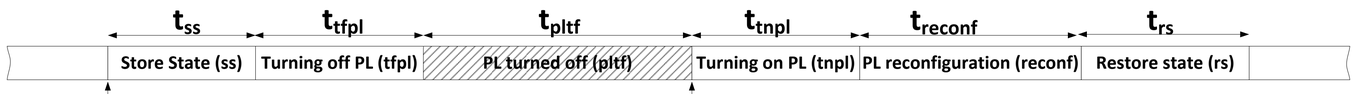


PL shut-down slop



Power versus V_{CCINT} voltage on ZC702

This section investigates the viability of physical power gating FPGA devices that incorporate a hardened processor in a different power domain. The run-time power gating approach is applied to Xilinx ZYNQ devices that incorporate a hardened Cortex A9 multi-processor.



Request for turning off the PL

$$P_{powerGating} = P_{ss} + P_{tfpl} + P_{pltf} + P_{tnpl} + P_{reconf} + P_{rs}$$

$$E_{powerGating} = t_{ss}.P_{ss} + t_{tfpl}.P_{tfpl} + t_{pltf}.P_{pltf} + t_{tnpl}.P_{tnpl} + t_{reconf}.P_{reconf} + t_{rs}.P_{rs}$$

$$E_{powerGating} < E_{plidle}$$

$$t_{ss}.P_{ss} + t_{tfpl}.P_{tfpl} + t_{pltf}.P_{pltf} + t_{tnpl}.P_{tnpl} + t_{reconf}.P_{reconf} + t_{rs}.P_{rs} < t_{plidle}.P_{plidle}$$

Request for turning on the PL

$$t_{plidle} > (t_{ss}.P_{ss} + t_{tfpl}.P_{tfpl} + t_{tnpl}.P_{tnpl} + t_{reconf}.P_{reconf} + t_{rs}.P_{rs})/P_{plidle}$$

$$t_{plidle} > t_{ss} + t_{tfpl} + t_{tnpl} + t_{reconf} + t_{rs}$$

Period	Time ($msec$)
Turn-off PL	4.84
Turn-on PL	4.84
Reconfiguration PL	87.3

	AXI-Timer	Motion Estimation	One-Microblaze	Five-Microblaze
Lower level time by Equ. 6	77.45	35.75	17.57	11.6 5
Lower level time by Equ. 5	95.55	95.55	95.55	95.55
Turn-off-efficiency time	95.55	95.55	95.55	95.55

	AXI-Timer	Motion Estimation	One-Microblaze	Five-Microblaze
Power of the PL in idle mode (W)	0.053	0.15	0.353	0.63
Power of the PL shut down (W)	0.0207	0.0207	0.0207	0.0207
Power reduction	60.9%	86.2%	94.1%	96.7%

The results show that the minimum time that the FPGA fabric must remain in power-off state for the technique to be energy efficient is in the order of milliseconds and up to 96% power reduction occurs when the fabric voltage is lowered below critical level.