Welcome to Heilbronn!

IWOCL 2026, May 6-8, 2026

10/06/26

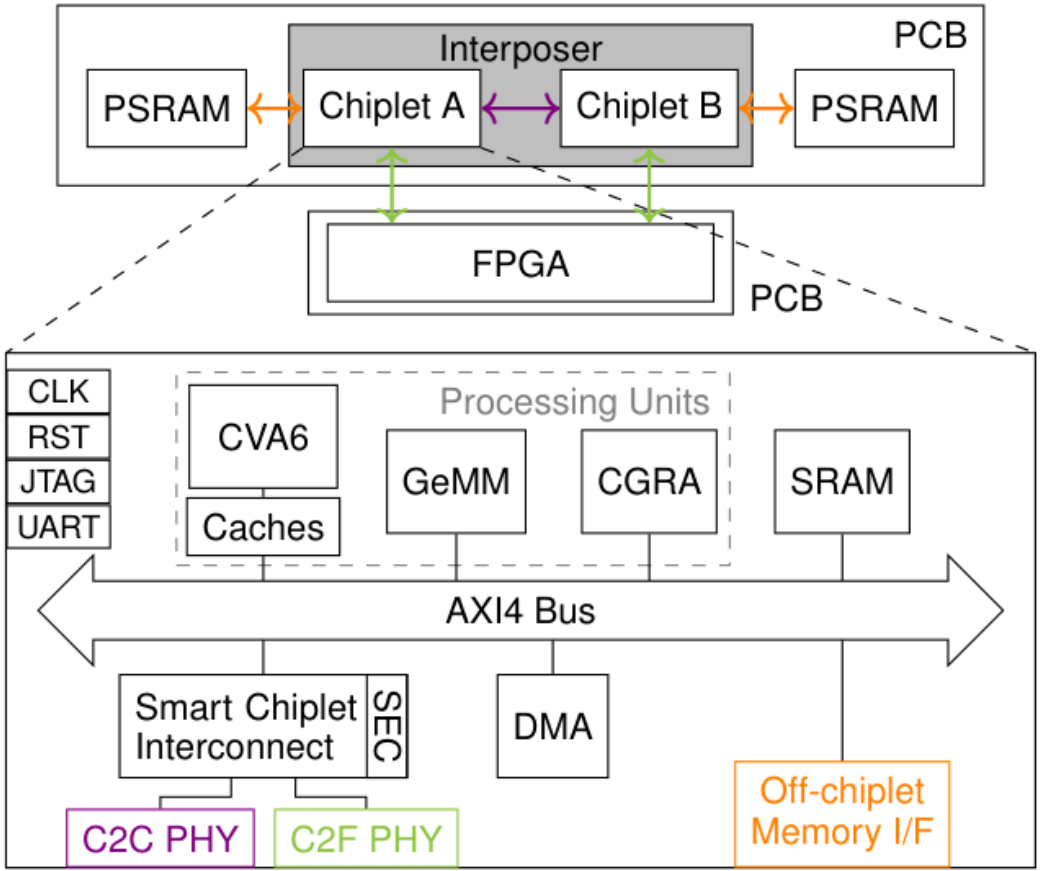
Carsten Trinitis & Hartwig Anzt

Professorship for Computer Architecture and Operating Systems (CAOS)
Campus Heilbronn

Technical University of Munich

Bavarian **C**hip-**D**esign **C**enter (BCDC aka AC⚡DC)

Edge AI Demonstrator



Dual-Chiplet Interposer Featuring

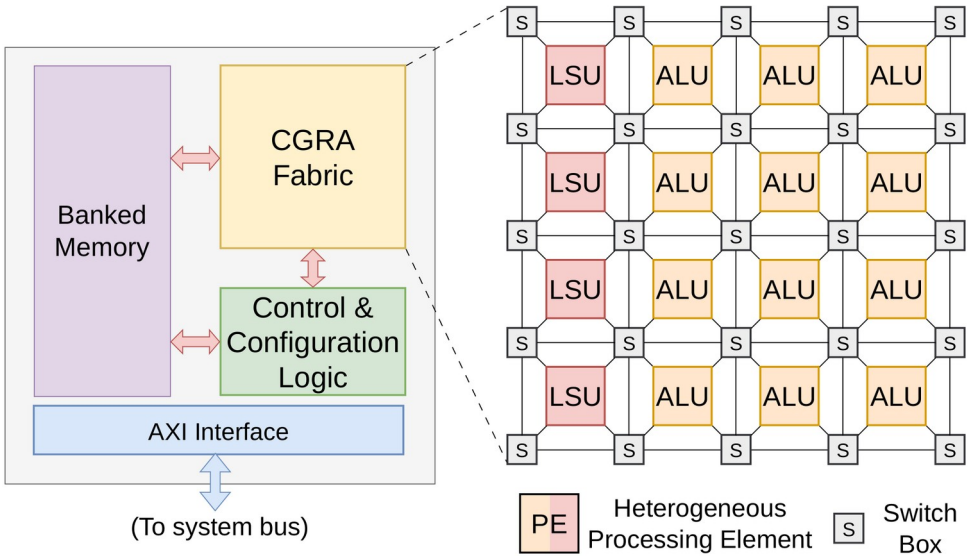
- Smart Chiplet Interconnect;
- Security Enhancement;
- Two Edge AI Accelerators:
  - Systolic Array for GeMM,
  - CGRA for Irregularities; →**by CAOS**
- Fused Compilation and Runtime.

Collaboration with six Chairs at TUM and Fraunhofer AISEC.

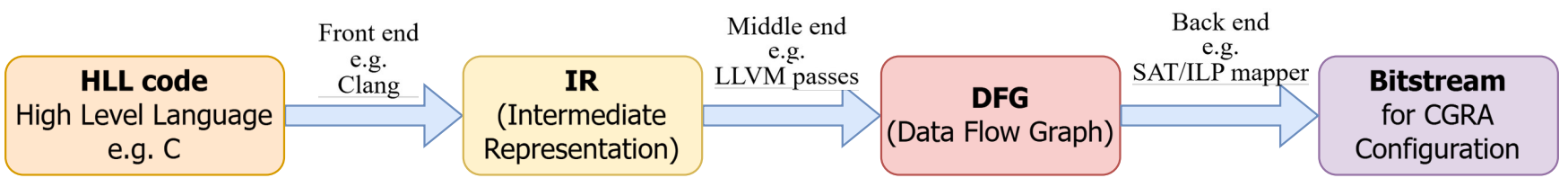
Chair for Computer Architecture and Operating Systems (CAOS)
TUM School of Computation, Information and Technology
Technical University of Munich Heilbronn

Bavarian **C**hip-**D**esign **C**enter (BCDC aka AC⚡DC)

Coarse **G**rained **R**econfigurable **A**rray for Edge AI by CAOS



- Highly parallel;
- Programmable;
- Lightweight and efficient for the Edge;
- Capable of irregular workloads.



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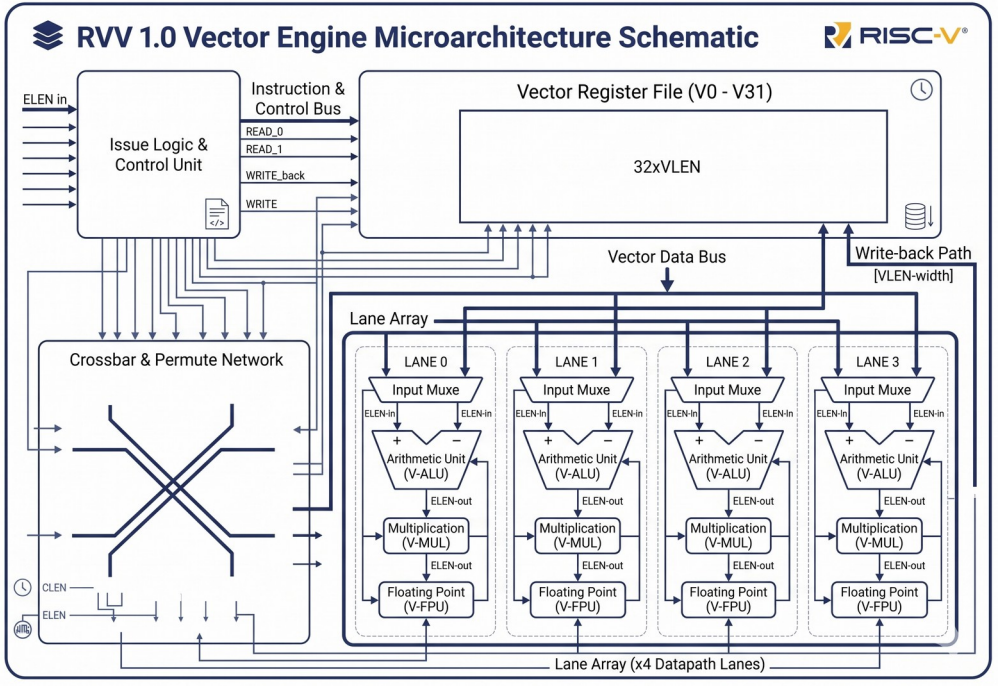
Custom ISA on RISC-V SIMD Architecture

Hardware-/Software Co-design:

Leveraging RISC-V Vector SIMD architecture to resolve efficiency bottlenecks.

- Flexible Scalability: Adapts instruction
- execution dynamically across various hardware vectors.
- SIMD Efficiency: Executes single instructions on multiple data points simultaneously for massive throughput.
- Hardware Agnostic: Bridges the performance gap between lightweight edge controllers and high-end processors.



Target Applications of HPC Infrastructure

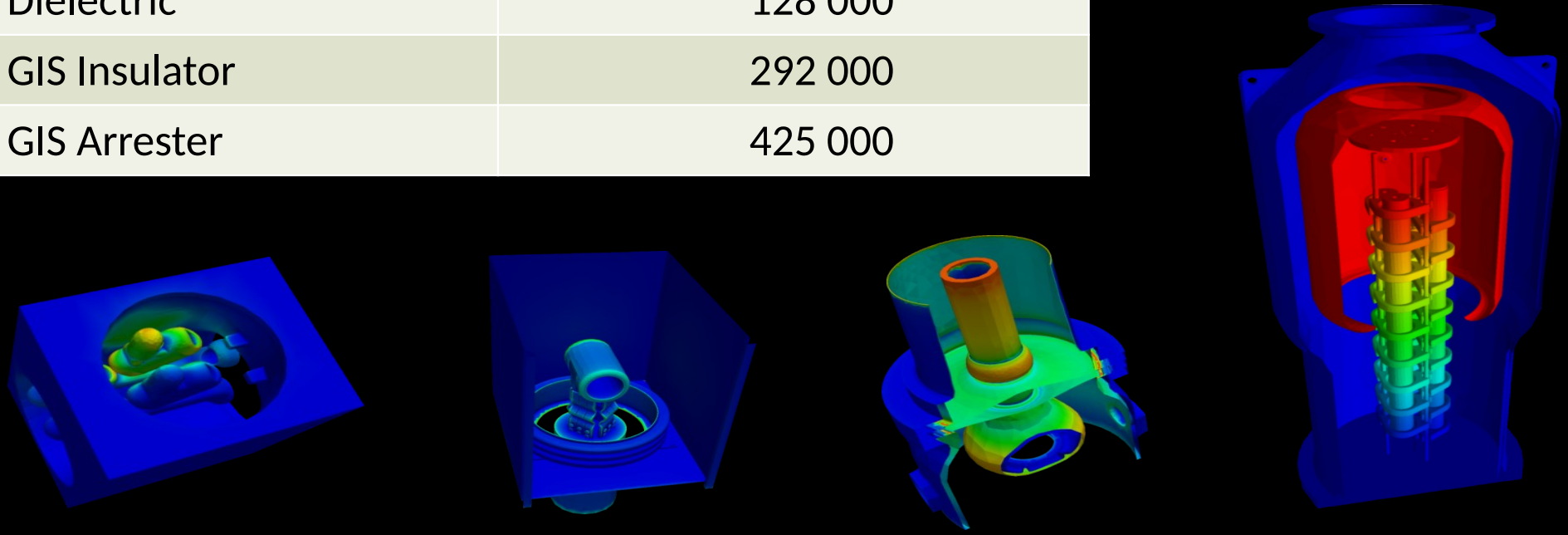
- SmartNIC Devices (Scale-up the computing clusters)
  - Delivering high-performance, programmable packet parsing MCU on NICs.
  - Customized vector operations allow network interfaces to rapidly process and route complex network traffic at line rate.

- Quantum Processors (Explore next generation computing system)
  - Addressing hundreds of Qubits simultaneously.
    By utilising a custom ISA framework layer, quantum controllers can execute precise, multi-qubit microwave control pulses synchronously.

- Maintain Standard Compliance
  - Enabling extreme custom performance scaling while maintaining absolute compliance with the standard RISC-V ISA.
    This ensures long-term software portability and leverages the global open-source compiler ecosystem.

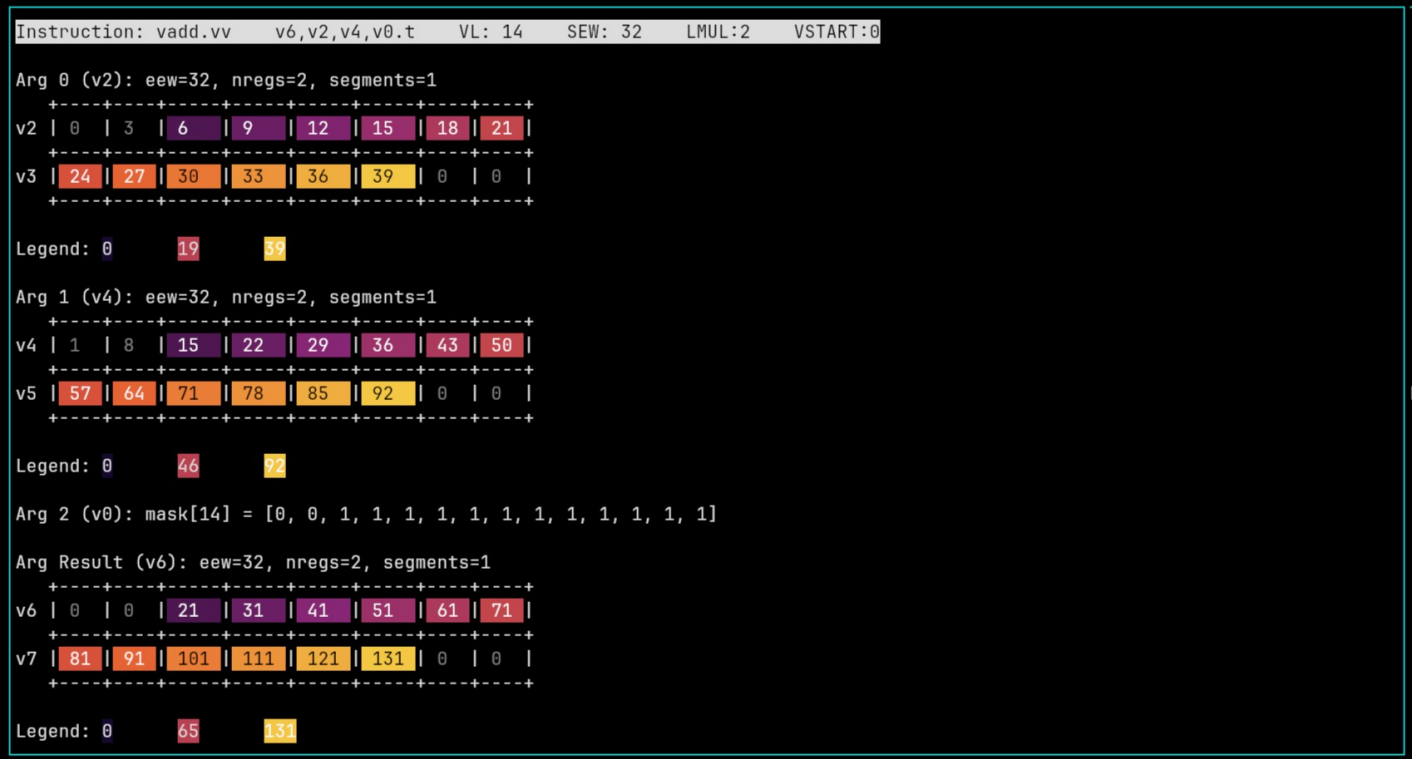
Electrostatic Field Simulation

Component	Matrix Size
EXK01	79 000
Dielectric	128 000
GIS Insulator	292 000
GIS Arrester	425 000



RISC-V Vector Debugger

- Extension of `gdb` wrt data parallelism.
- As part of the DARE-EU project.
- TUM’s part: Parallel debugger as part of the RISC-V HPC ecosystem.




```
24
25   uintptr_t stride = 4;    // bytes for e32
26   uint32_t  sA = 5;
27   uint32_t sB = 0x5a;
28 printf("%#" PRIx64 "\n", a);
29   // ---------------- Block 1: config + arith/logic + unit/strided/indexed/seg memory ----------------
B+>  30 asm volatile(
31   "vsetvli     t0, %[avl], e32, m2, ta, ma\n\t"
32
33   // Load inputs
34   "vle32.v     v2,  (%[pa])\n\t"
35   "vle32.v     v4,  (%[pb])\n\t"
36
37   // Build a mask
38   "vmsge.vi    v0,  v2, 5\n\t"
```

```
   0x2aaaaaa76c <rvv_viz_mix+116>  addi    a1,a1,4
   0x2aaaaaa76e <rvv_viz_mix+118>  addi    a2,a2,2
   0x2aaaaaa770 <rvv_viz_mix+120>  bne     a5,t4,0x2aaaaaa748 <r
   0x2aaaaaa774 <rvv_viz_mix+124>  auipc   s5,0x3
   0x2aaaaaa778 <rvv_viz_mix+128>  addi    s5,s5,-1268
   0x2aaaaaa77c <rvv_viz_mix+132>  li      a2,32
   0x2aaaaaa780 <rvv_viz_mix+136>  li      a1,170
   0x2aaaaaa784 <rvv_viz_mix+140>  mv      a0,s5
   0x2aaaaaa786 <rvv_viz_mix+142>  jal     0x2aaaaaa5f0 <memset@
   0x2aaaaaa78a <rvv_viz_mix+146>  auipc   a2,0x2
   0x2aaaaaa78e <rvv_viz_mix+150>  addi    a2,a2,-1802
   0x2aaaaaa792 <rvv_viz_mix+154>  auipc   a1,0x0
   0x2aaaaaa796 <rvv_viz_mix+158>  addi    a1,a1,302
   0x2aaaaaa79a <rvv_viz_mix+162>  li      a0,2
   0x2aaaaaa79c <rvv_viz_mix+164>  jal     0x2aaaaaa5e0 <__print
B+ 0x2aaaaaa7a0 <rvv_viz_mix+168>  li      a5,5
   0x2aaaaaa7a2 <rvv_viz_mix+170>  li      a4,4
   0x2aaaaaa7a4 <rvv_viz_mix+172>  li      a3,90
   0x2aaaaaa7a8 <rvv_viz_mix+176>  vsetvli t0,s0,e32,m2,ta,ma
   0x2aaaaaa7ac <rvv_viz_mix+180>  vle32.v v2,(s1)
   0x2aaaaaa7b0 <rvv_viz_mix+184>  vle32.v v4,(s2)
   0x2aaaaaa7b4 <rvv_viz_mix+188>  vmsgt.vi        v0,v2,4
   0x2aaaaaa7b8 <rvv_viz_mix+192>  vmsne.vi        v1,v4,0
   0x2aaaaaa7bc <rvv_viz_mix+196>  vmand.mm        v0,v0,v1
   0x2aaaaaa7c0 <rvv_viz_mix+200>  vadd.vv v6,v2,v4,v0.t
  >0x2aaaaaa7c4 <rvv_viz_mix+204>  vsub.vx v6,v6,a5,v0.t
   0x2aaaaaa7c8 <rvv_viz_mix+208>  vmul.vv v8,v2,v4,v0.t
   0x2aaaaaa7cc <rvv_viz_mix+212>  vand.vv v8,v8,v6,v0.t
   0x2aaaaaa7d0 <rvv_viz_mix+216>  vor.vx  v10,v8,a5
   0x2aaaaaa7d4 <rvv_viz_mix+220>  vxor.vx v10,v10,a3
(gdb) r
Starting program: /u/home/schaeffj/demo
[Thread debugging using libthread_db enabled]
Using host libthread_db library "/lib/riscv64-linux-gnu/libthread
_db.so.1".

Breakpoint 1, rvv_viz_mix (avl=avl@entry=14) at test_viz.c:30
(gdb) vstep
(gdb) vstep
(gdb) vstep
(gdb) vstep
(gdb) vstep
(gdb) vstep
(gdb) vstep
(gdb) vcolor relative
vcolor: color_mode=relative, only_color=False
(gdb)
```

Organisational Issues

- Lunch will be served in the entrance hall (for exact times see programme!).
- Talks will be held in D.1.07 / D.1.08 (i.e. here :)).
- For anything else follow the sings or ask the organisers.

Enjoy IWOCL 2026 and Heilbronn!