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SYCL for Xilinx Versal ACAP AIE CGRA
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Abstract
SYCL is a single-source C++ DSL targeting a large variety of accelerators in a unified way by using different backends.
Xilinx Versal ACAP is a new system-on-chip (SoC) device integrating various computing resources like various CPUs, an FPGA, a coarse-grain reconfigurable array (CGRA), etc. interconnected by different network-on-chip (NoC).
The AIE CGRA is an array of 400 VLIW DSPs operating on 512-bit vectors with their own neighborhood distributed memory (32 KiB data, 16 KiB instruction).
We expose architectural details to the programmer through some SYCL extensions and extend SYCL with a geographical collective model.
The SYCL implementation targeting the AIE CGRA by merging 2 different open-source implementations, Intel’s oneAPI DPC++ with some LLVM passes from triSYCL and a new SYCL runtime from triSYCL.
The SYCL device compiler generates LLVM IR for the Synopsys ASIP CHESS compiler generating the AIE target binaries.

Weaving heterogeneous tiles and memories with meta-programming

```
#include <iostream>

int main() {
    std::cout << "Hello, I am the AIE tile (" << th.x() << ", " << th.y() << ")\n" << std::endl;
    return 0;
}
```

Type-safe access to heterogeneous neighbor memories (PDE, stencil...)

```
auto own = t::mem();
for (int i = 0; i < image_size; ++i) {
    auto north = own.w[j][i + 1] - own.w[j][i];
    // Compute dw/dx
    own.w[j][i] -= north / alpha;
}
```

Different multi-level implementation/emulation for hardware-software co-design

```
// A program tile has to inherit from acap::aie::tile<AIE, X, Y>
tile_prog : acap::aie::tile<AIE, X, Y>
```

Implementation

```
#include <iostream>

int main() {
    std::cout << "Hello, I am the AIE tile (" << th.x() << ", " << th.y() << ")\n" << std::endl;
    return 0;
}
```

Conclusion

```
#include <iostream>

int main() {
    std::cout << "Hello, I am the AIE tile (" << th.x() << ", " << th.y() << ")\n" << std::endl;
    return 0;
}
```

Retargetable to other CGRAs