Modeling Heterogeneous Computing Performance with Offload Advisor



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Agenda

- Introduction to Offload Advisor
- Command line tips
- Understanding the performance modelization
- GPU Roofline Analysis



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Introduction to Offload Advisor



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Intel Offload Advisor (Beta)



- Helps defining which sections of the code should run on a given accelerator
- Provides performance projection on accelerators (currently gen9 and gen11)

Intel® Advisor Beta OFFLOAD ADVISOR Summary Offloaded Regions N	on Offloaded Regions Call Tree Configurati	on Logs		Speed Up for Accelerated Code (7) 8	3.9x Number of Offic	ads @ 1 Fraction	Intel® Advisor Beta, build 604296 of Accelerated Code @ 99%
Program metrics ⑦				Offloads bounded by ⑦		Gen9 GT2 configur	ation (?) 🛃 🖞 🖒
Original Ø 13.84s Accelerated Ø 1.63s Target Platform Gen9 GT2 Number of Offloads Ø 1 Speed Up for Accelerated Code Ø 8.9x Amdahi's Law Speed Up Ø 8.5x Fraction of Accelerated Code Ø 99%	Invocation Tax @	0.09s 1.54s 0s <0.01s <0.01s	34 5	Compute Ø 0% I.3 Cache BW Ø 0% LLC BW Ø 99% Memory BW Ø 0% Data Transfer Ø 0% Dependency Ø 0% Trip Count Ø 0% Non Offloaded Ø <1%	0	1 15 GHz frequency © 24 EU © 512 0 KB L3 © 208 GB/s L3 bandwidth © 24 GB/s DRAM bandwidth © 1 Integrated GPU ©	
Top offloaded ⑦	Speed Up @	Bounded By Ø	Data Transfer @	Top non offloaded ⑦	Data Transfer @	execution Time @	Why Not Offloaded @
[loop in iso_3dfdSompSparallel@52 at iso- 3dfd_parallel.cc:53]	8.94x CPU 13.75s GPU 1.54s	LLC_BW		[loop in iso_3dfd at iso-3dfd_parallel.cc:85]	0.09MB	CPU 13.75s GPU 19.45s	Not profitable.
				[loop in main at iso-3dfd_main.cc:194]	0MB	CPU 0.02s GPU <0.01s	Total time is too small for reliable modelling. Useloop-filter-threshold=0 to model such small offloads.
				[loop in initialize at iso-3dfd_main.cc:59]	OMB	CPU 0.02s GPU <0.01s	Total time is too small for reliable modelling. Useloop-filter-threshold=0 to model such small offloads.
				[loop in initialize at iso-3dfd_main.cc:60]	омв	CPU 0.02s GPU <0.01s	Total time is too small for reliable modelling. Useloop-filter-threshold=0 to model such small offloads.



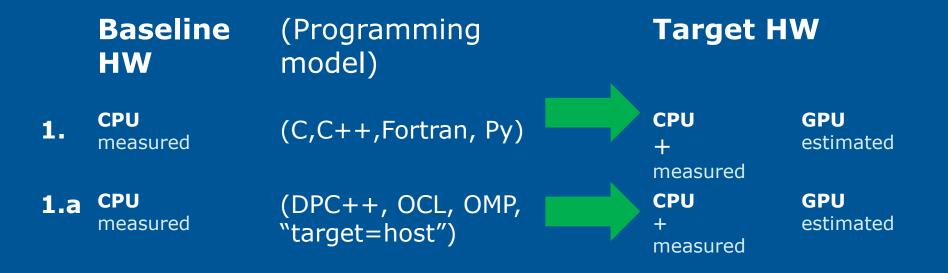
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Modeling Flows supported: NOW





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Modeling Flows supported: NOW + Coming Soon

	Baseline HW	(Programming model)	Target HW			
1.	CPU measured	(C,C++,Fortran, Py)	CPU + measured	GPU estimated		
1. a	CPU measured	(DPC++, OCL, OMP, "target=host")	CPU + measured	GPU estimated		
2	CPU+iGPU measured	(C, C++, Fortran, DPC++, OCL, OMP)	CPU + measured	GPU estimated		



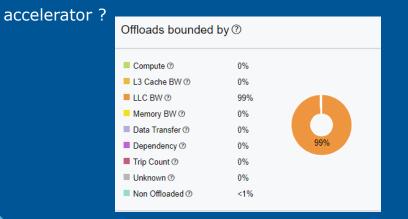


From Your CPU Application, you wonder:

How your code might perform on an accelerator ?

Program metric	Program metrics ⑦								
Original ⑦ Accelerated ⑦ Target Platform	13.84s 1.63s	Gen9 GT2	Time on Host ⑦	0.09s					
Number of Offloads ⑦ 1 Speed Up for Accelerated Code ⑦ 8.9x Amdahl's Law Speed Up ⑦ 8.5x Fraction of Accelerated Code ⑦ 99%		 Time on Accelerator ⑦ Data Transfer Tax ⑦ Invocation Tax ⑦ Code Transfer Tax ⑦ 	1.54s 0s <0.01s <0.01s	94%					

• What might be limiting your performance on the





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• What should you offload ?

Top offloaded ⑦									
Location ⑦	Speed Up ⑦		Bounded By ⑦	Data Transfer @					
[loop in iso_3dfd\$omp\$parallel@52 at iso- 3dfd_parallel.cc.53]	8.94x _	CPU 13.75s GPU 1.54s	LLC_BV	/ <0.01MB					

What are the bad candidates for offload and Why ?

Top non offloaded ③									
Location ⑦	Data Transfer @	Execution Time (?)			Why Not Offloaded @				
[loop in iso_3dfd at iso-3dfd_parallel.cc:85]	0.09MB	-	CPU GPU	13.75s 19.45s	Not profitable.				
[loop in main at iso-3dfd_main.cc:194]	0MB	-	CPU GPU	0.02s <0.01s	Total time is too small for reliable modelling. Useloop-filter-threshold=0 to model such small offloads.				



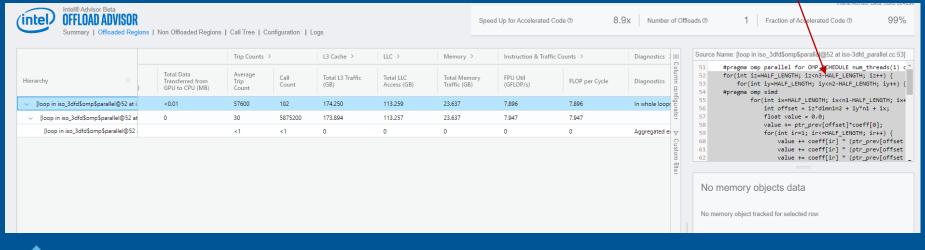
Top Offloaded in depth



This is where you will use DPCPP or

OMP target for offload

- Provides a detailed description of each loop interesting for offload
 - Timings (total time, time on the accelerator, speedup)
 - Offload metrics (offload taxe, data transfers)
 - Memory traffic (DRAM, L3, L2, L1), trip count
 - Highlight which part of the code should run on the accelerator





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Non Offloaded in depth



- Explains why Advisor doesn't recommend a given loop for offload
 - Dependency issues
 - Not profitable
 - Total time is too small



Intel® Advisor Beta OFFLOAD ADVISOR

Speed Up for Accelerated Code (7) 8.9

8.9x Number of O

Summary | Offloaded Regions | Non Offloaded Regions | Call Tree | Configuration | Logs

	Information >				Potential Offload <				
Hierarchy	oop ion ed?	Estimated Execution Time on Accelerator (+Host) (s)	Bounded By	Fraction Offloaded (%)	Why Not Offloaded	Potential Spee Up for Whole Region			
[loop in iso_3dfd at iso-3dfd_parallel.co	:	1.539		100.00	Not profitable.	0.7068x	igura		
[loop in main at iso-3dfd_main.cc:194]		0.020		0	Total time is too small for reliable modelling. Useloop-filter-threshold=0 to model such small offloads.	41338.1565x	tor		
> [loop in initialize at iso-3dfd_main.cc:59	9				Total time is too small for reliable modelling. Useloop-filter-threshold=0 to model such small offloads.	640.4016x	∇		
							2		



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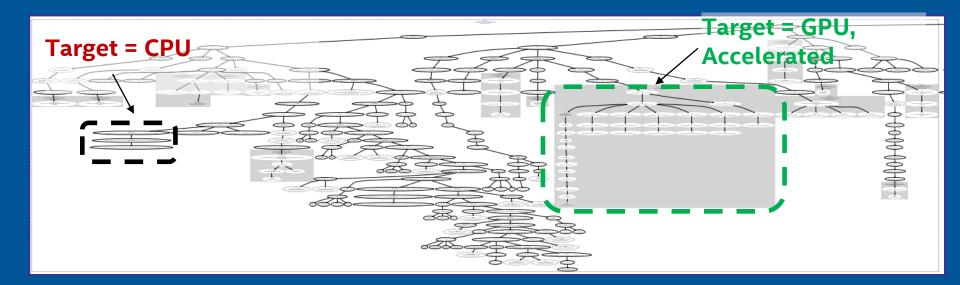
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Program Tree



• The program tree offers another view of the proportion of code that can be offloaded to the accelerator.





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Command Line Tips



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Before you start to use Offload Advisor

 The only strict requirement for compilation and linking is full debug information:

-g: Requests full debug information (compiler and linker)

 Offload Advisor supports any optimization level, but the following settings are considered the optimal requirements:

-02: Requests moderate optimization

-no-ipo: Disables inter-procedural optimizations that may inhibit Offload Advisor to collect performance data (Intel® C++ & Fortran Compiler specific)





Source Offload Advisor



 To set up the Intel® Advisor Beta environment, run one of the shell script:

source <ONEAPI_INSTALL_DIR>/setvars.sh

or

source <ADV_INSTALL_DIR>/env/vars.sh

- This script sets all required Intel Advisor environment variables, including APM, which points to <adv_INSTALL_DIR>/perfmodels
- This is the location of the Offload Advisor scripts in the Intel® Advisor Beta installation directory



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The performance modeling functionality is available on Linux* OS only



How does it work ?



Easy to collect data and generate output with batch mode:

advixe-python <ADV_INSTALL_DIR>/perfmodels/run_oa.py
<path_to_result_dir> -config gen9 --out-dir <path_to_result_dir> [-options] -- <app>

- By default, run_oa.py marks up all regions and only selects the most profitable ones for analysis
- To generate the report.html, uses the following command:

advixe-python \$APM/analyse.py <project_dir> --config gen9 [--options] --<app_binary> [app_options]

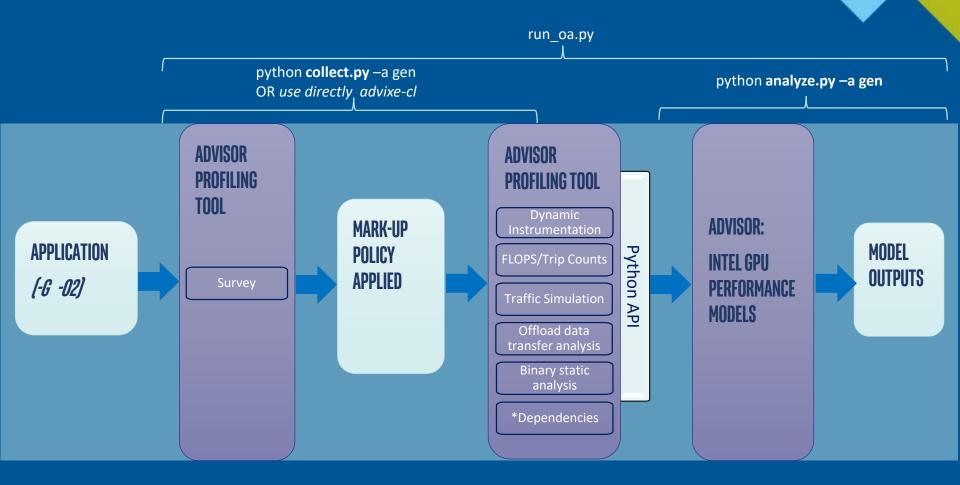
u31313@s001-n004:/opt/intel/inteloneapi/advisor/latest/perfmodels\$ ls										
accelerators	analyze.py	collect.py	debug.so	environ.py	oa_wrapper.so	shared.so	toml			
analyze_impl.so	collect_impl.so	compute_stats.py	dot_graph.so	helpers	run_oa.py	template	tree.so			







Run_oa.py: What is running behind?





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Offload advisor Output Overview

- report.html: Main report in HTML format
- report.csv and whole_app_metric.csv: Comma-separated CSV files
- program_tree.dot: A graphical representation of the call tree showing the offloadable and accelerated regions
- program_tree.pdf: A graphical representation of the call tree

Generated if the DOT(GraphViz*) utility is installed

1:1 conversion from the program_tree.dot file

 JSON and LOG files that contain data used to generate the HTML report and logs, primarily used for debugging and reporting bugs and issues





Want to avoid dependency checking?

- Dependency adds a lot of time to the collection and you might want to remove it.
- Add the option -c basic for the collection:

advixe-python <ADV_INSTALL_DIR>/perfmodels/run_oa.py
<path_to_result_dir> -config gen9 -c basic --out-dir
<path_to_result_dir> [--options] -- <app>

• Add the option --assume-parallel for the analysis:

advixe-python \$APM/analyse.py <project_dir> --assume-parallel --config
gen9 [--options] -- <app_binary> [app_options]







Understanding the performance modelization



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The mechanisms behind 1/2

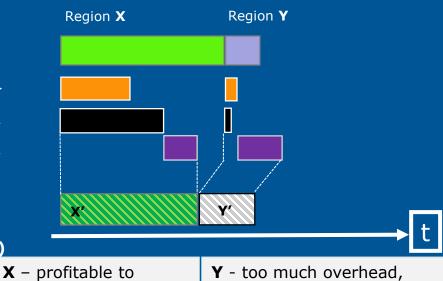
First order analytical modeling pillars:

- Compute throughput model
- Memory sub-system model
- Offload data transfer modeling

Execution time on baseline platform (CPU)



- Execution time on accelerator. Estimate
 assuming bound exclusively by caches/memory
- Offload Tax estimate (data transfer + invoke)



Final estimated time on target platform (eg GPU)

X – profitable to accelerate, t(X) > t(X')

= max($t_{\text{compute}}, t_{\text{memory subsystem}}$) + $t_{\text{data transfer tax}} + t_{\text{kernel launch}}$

Y - too much overhead, not accelerable, t(Y) < t(Y')

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t region



The mechanisms behind 2/2

We minimize the total time spent in this loop hierarchy by varying offload strategies U (offload/non-offload, #threads for each component $loop_i$ of loopnest)

Objective function: $T_{all} = \min_{U = \{uf_1, uf_2, ...\}} (\sum_i T_i + t_{data \ transfer} + t_{invoke} + T_{cpu})$

$$T_{i} = max \begin{cases} T_{i}^{Comp_only}() \\ T_{i}^{M_{k_oonly}}(M_{i}^{k}) = \frac{M_{i}^{k}}{BW_{k}} \end{cases}$$

This is effectively "balance" (throughput) model

Reject loopnests for which $T(x86) / T_{all}(x86+"X") < 1.0$

Under algorithmic constraints (Dependencies and TripCount/Granularity)



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GPU Roofline Analysis



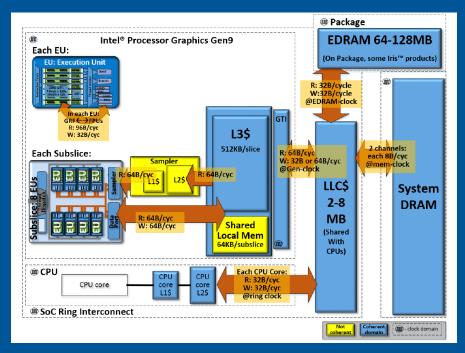
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Intel® Gen9 Memory Hierarchy

- Intel® Graphics Compute Architecture uses the same DRAM with the CPU
- Level-3 (L3) data cache: slice-shared asset
- Shared Local Memory (SLM): a dedicated structure within the L3 that supports the work-group local memory address space
- Graphics Technology Interface (GTI): a dedicated interface unit connects the entire architecture interfaces to the rest of the SoC components
- The rest of SoC memory hierarchy includes the large Last-Level Cache (LLC, which is shared between CPU and GPU), possibly embedded DRAM and finally the system DRAM



A view of the SoC chip level memory hierarchy and its theoretical peak bandwidths for the compute architecture of Intel processor graphics gen9



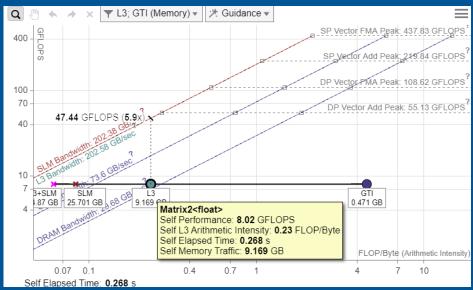
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Find Effective Optimization Strategies

GPU Roofline Performance Insights

- Highlights poor performing loops
- Shows performance 'headroom' for each loop
 - Which can be improved
 - Which are worth improving
- Shows likely causes of bottlenecks
 - Memory bound vs. compute bound
- Suggests next optimization steps





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How to run?

The Roofline model on GPU is a technical preview feature and is not available by default.

To enable it:

export ADVIXE_EXPERIMENTAL=gpu-profiling

To run the GPU Roofline analysis in the Intel® Advisor CLI:

Run the Survey analysis with the --enable-gpu-profiling option:

advixe-cl -collect=survey --enable-gpu-profiling --project-dir=<my_project_directory> --search-dir src:r=<my_source_directory> -- ./myapp [app_parameters]

Run the Trip Counts and FLOP analysis with --enable-gpu-profiling option:

advixe-cl -collect=tripcounts --stacks --flop --enable-gpu-profiling --project-dir=<my_project_directory>
--search-dir src:r=<my_source_directory> -- ./myapp [app_parameters]

Generate a GPU Roofline report: advixe-cl --report=roofline --gpu --project-dir=<my_project_directory> --report-output=roofline.html

Open the generated roofline.html in a web browser to visualize GPU performance.



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Roofline Analysis on Intel® GPU

▼ Default: GTI (Memory) ▼ N Q 🔭 Guidance 🔻 SP Vector FMA Peak: 437.83 GELOPS GFLOPS 400 335.69 G SP Vector Add Peak: 219.84 GFLOPS DP Vector FMA Peak: 108.62 GFLOPS 100 70 DP Vector Add Peak: 55.13 GFLOPS 55.13 GFLOPS (6.9x)-40 L3 Bandwidth: 202 58 GBISec SLM Bandwidth. 202.38 GBIsec 10 7 GTI Bandwidth: Matrix2<float> 4 DRAM Bandwidth: 29.68 Self Performance: 8.02 GFLOPS Self GTI Arithmetic Intensity: 4.56 FLOP/Byte Self Elapsed Time: 0.268 s Self Memory Traffic: 0.471 GB 0.07 0.1 0.4 0.7 4 7 10 1



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Roofline Chart from the Intel Advisor



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